SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)

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R. V. S NAGAR CHITTOOR-517 127

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LABORATORY MANUAL

LAB CODE : 20AEC28

LAB NAME : DIGITAL COMMUNICATIONS

LABYEAR & SEMESTER : III - I

REGULATIONS : R-20

Prepared by

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SVCET(A).

20AEC28 – DIGITAL COMMUNICATIONS LAB

SYLLABUS

Course Outcomes: After completion of the course, the students will be able to

CO1: Analyze different coding techniques in digital communications.

CO2: Demonstrate sampling theorem and different modulation and demodulation schemes.

LIST OF EXPERMENTS
(Minimum Ten Experiments has to be conducted)

1. Generation of Various Encoding Schemes
2. Pulse Code Modulation and Demodulation.
3. Sampling Theorem – Verification.
4. Delta modulation and Demodulation.
5. Amplitude shift keying - Modulation and Demodulation.
6. Frequency shift keying - Modulation and Demodulation.
7. Phase shift keying - Modulation and Demodulation.
8. Differential phase shift keying - Modulation and Demodulation.
9. QPSK - Modulation and Demodulation.
10. DQPSK - Modulation and Demodulation.
11. Binary Phase Shift Keying - Modulation and Demodulation.
12. Differentially Encoded Phase Shift Keying - Modulation and Demodulation.

INDEX

Sl. No	Date	NAME OF THE EXPERIMENT	Pg. No.	Faculty Signature

Exp. No. :1 **Date:**

GENERATION OF VARIOUS ENCODING SCHEMES

AIM : To generation Unipolar NRZ, Polar NRZ, Unipolar RZ andPolar RZ line code.

EQUIPMENTS :

APPARATUS	RANGE	QUANTITY
Data encoding Trainer Kit		1
Digital storage oscilloscope	100MHz, 1GSa/S	1
Power supply		1
Probes		As per req.
Patch cord		As per req.
Connecting wires		As per req.

THEORY:

"1" and "0" can be represented in various formats in different levels and waveforms. The selection of coding technique depends on system band width, system ability to pass dc level information, error checking facility.

Non return to Zero (level): The NRZ(L) waveform simply goes low for one bit time to represent a data "0" and high to represent data "1".For lengthy data the clock is lost in asynchronous mode. The maximum rate at which NRZ can change is half the data clock, when alternate 0"s and 1"s are there.

DC Level: A length data will have only a dc level as its waveform, a dc voltage cannot be used in circuits which involve transformers like telephone, AC coupled amplifiers, capacitors, filter etc.

Manchester Bi-phase : „0" is encoded low during first half of bit time & high for other half of bit & vice versa for „1".There is no synchronization problem in the receiver. It is independent of DC levels, since there is a transition occurring in each bit. Its max frequency is equal to data clock rate. There is at leastone transition per bit. Since there is midway transition, it makes clock regeneration difficult so we use special bi phase clock recovery circuit.

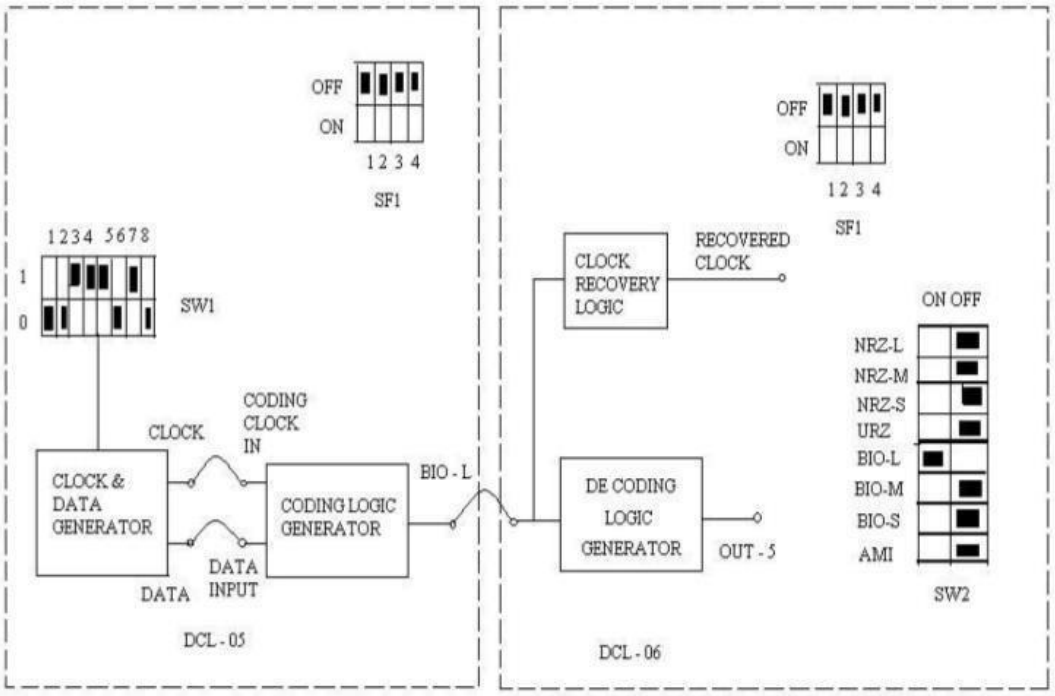
Return to Bias: It is a 3 level code, consists of positive, negative and zero. Easy clock synchronization is possible."1" for positive,"0" for negative in first half and zero bias for second half. Maximum frequency isequal to data clock frequency. A DC level of waveforms depends on strings of 1"s and 0"s.Hence we cannot use AC coupled communication link. Timing information is easily obtained. The system isreferred to as „self-clocking system", as magnitude of waveform is original data signal. It requires complex transmitters

PROCEDURE:

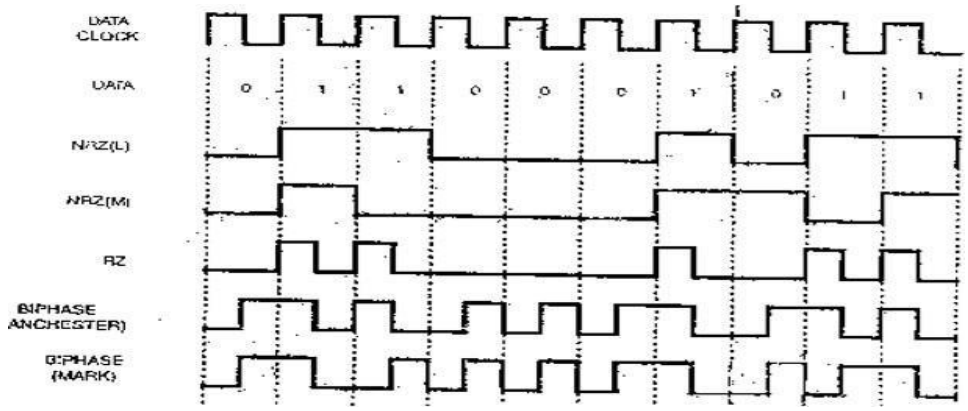
1. Connect the data generator output to code generator kit. This gives the random binary sequencetothe kit.
2. Connect the clock signal to the trainer kit.

3. Connect the output to the DSO channel along with the clock signal.
4. Observe the waveforms with respect to clock on a dual channel CRO, and compare with themodelgraph.
5. Plot the waveforms for different codes.

BLOCK DIAGRAM/ CIRCUIT DIAGRAM:



GRAPH:



OBSERVATION:

Signal	Amplitude	Time period
Input		
Output		

RESULT:

Exp.No:2 **Date:**

PULSE CODE MODULATION AND DEMODULATION

AIM : To Study the generation and detection of Pulse Code Modulation (PCM).

EQUIPMENT :

APPARATUS	RANGE	QUANTITY
PCM modulation and demodulation trainer kit		1
Digital storage oscilloscope	100MHz, 1GSa/S	1
Power supply		1
Probes		As per req.
Patch cord		As per req.
Connecting wires		As per req.

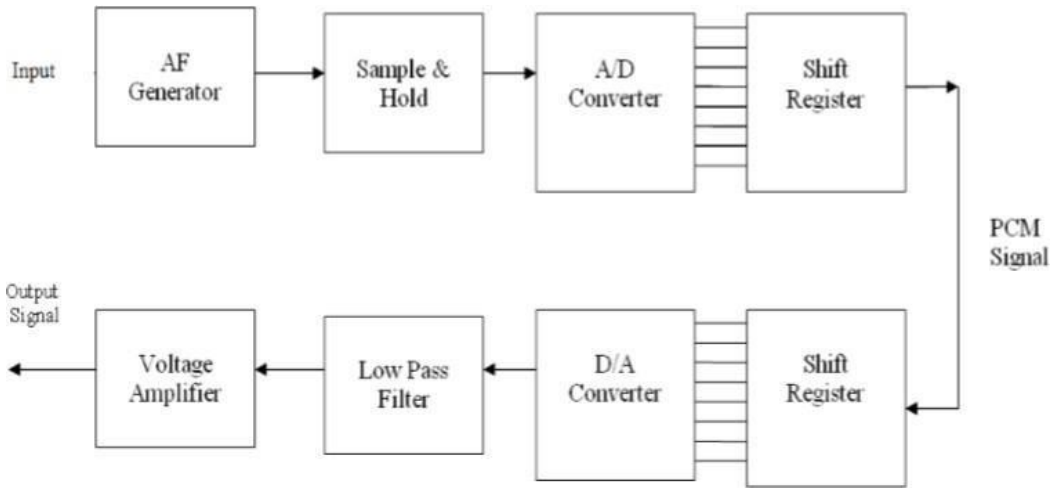
THEORY:

In Pulse code modulation (PCM) only certain discrete values are allowed for the modulating signals. The modulating signal is sampled, as in other forms of pulse modulation. But any sample falling within a specified range of values is assigned a discrete value. Each value is assigned a pattern of pulses and the signal transmitted by means of this code. The electronic circuit that produces the coded pulse train from themodulating waveform is termed a coder or encoder. A suitable decoder must be used at the receiver inorderto extract the original information from the transmitted pulse train.

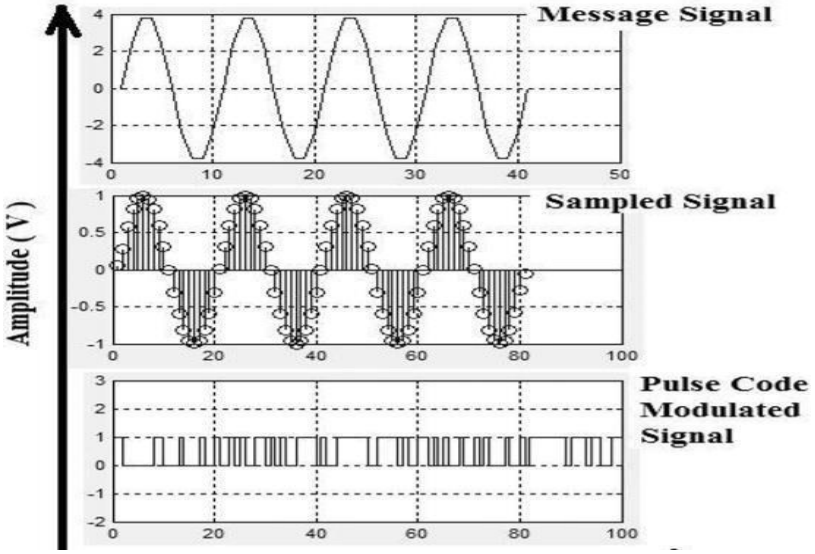
PROCEDURE:

1. Make the connections as per the diagram as shown in the Fig.1.and switch on the power supply of the trainer kit.
2. Clock generator generates a 20 KHz clock .This can be given as input to the timing and control circuitand observe the sampling frequency fs= 2 KHz approximately at the output of timing and control circuit.
3. Apply the signal generator output of 6V(p-p) approximately to the A to D converter input and notedown the binary word from LED‟s i.e. LED “ON” represents „1‟ & “OFF” represents „0‟.
4. Feed the PCM waveform to the demodulator circuit and observe the waveform at the output of D/Awhich is quantized level.

BLOCK DIAGRAM/ CIRCUIT DIAGRAM:



GRAPH:



OBSERVATION:

SIGNAL	AMPLITUDE(v)	TIME PERIOD	FREQUENCY
Message signal			
Clock signal			
PCM modulate doutput			
Demodulated signal			

RESULT:

Exp:3 **Date:**

SAMPLING THEOREM – VERIFICATION

AIM: To verify sampling theorem.

EQUIPMENTS

- Experimenter kit DCL –01.
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

The kit is used to study Analog Signal Sampling and its Reconstruction. It basically consists of functional blocks, namely Function Generator, Sampling Control Logic, Clock section, Sampling Circuitry and Filter Section.

Function Generator

This Block generates two sine wave signals of 1 KHz and 2 KHz frequency. This sine wave generationis done by feeding 16 KHz and 32 KHz clock to the shift register. The serial to parallel shift register with the resistive ladder network at the output generates 1 KHz and 2 KHz sine waves respectively by the serial shift operation. The R-C active filter suppresses the ripple and smoothness the sine wave. The unity gain amplifier buffer takes care of the impedance matching between sine wave generation and sampling circuit.

Sampling Control Logic

This unit generates two main signals used in the study of Sampling Theorem, namely the analog signals (5V pp, frequency 1KHz and 2KHz) & sampling signal of frequency 2KHz, 4KHz, 8KHz, 16KHz, 32KHz, and 64KHz. The 6.4 MHz Crystal Oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies from 2 KHz to 64KHz and the other control frequencies.

From among the various available sampling frequencies, required sampling frequency is selected by using the Frequency selectable switch. The selected sampling frequency is indicated by means of corresponding LED.

BLOCK DIAGRAM

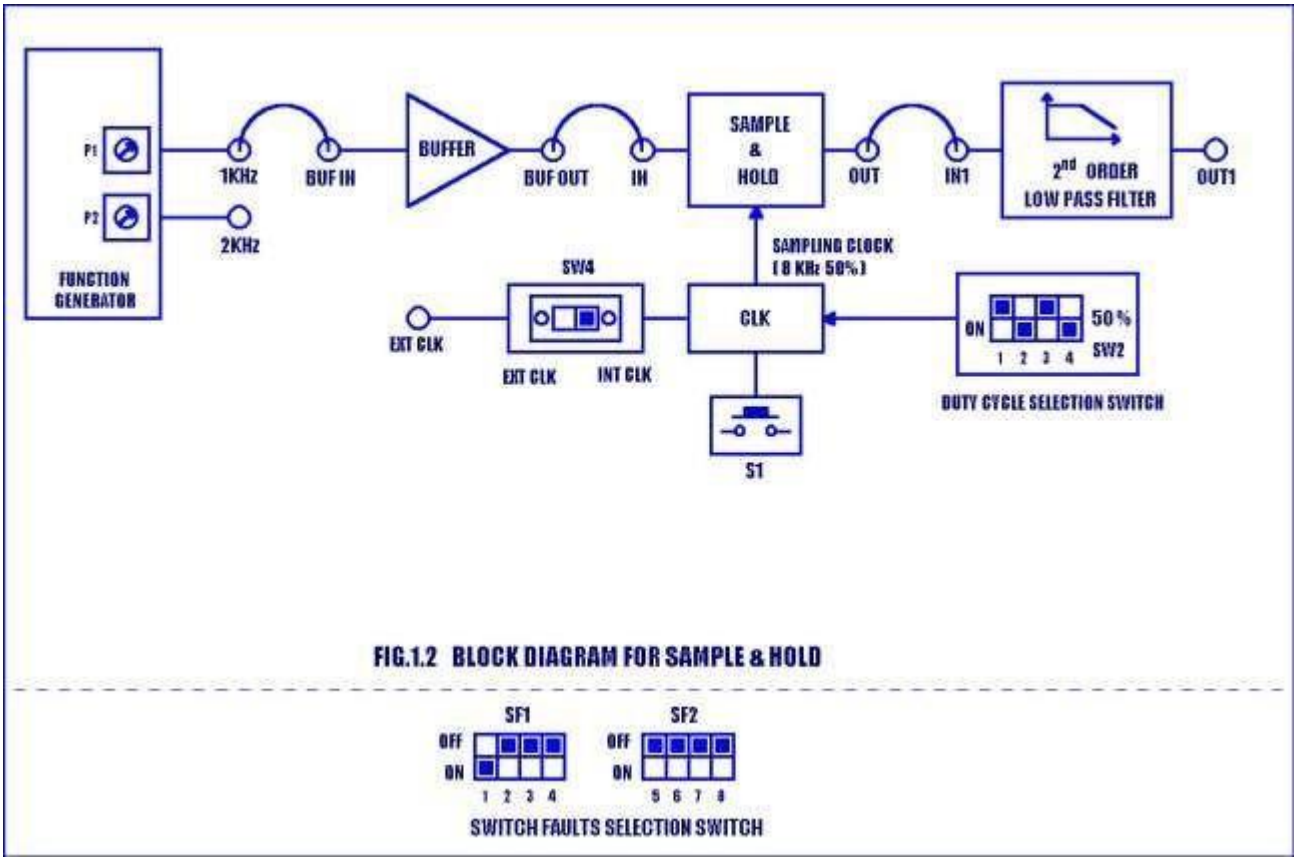


FIG.1.2 BLOCK DIAGRAM FOR SAMPLE & HOLD

Clock Section

This section facilitates the user to have his choice of external or internal clock feeding to the sampling section by using a switch (SW4).

Sampling Circuitry

The unit has three parts namely, Natural Sampling Circuit, Flat top Sampling Circuit, and Sample andHold Circuit.

The Natural sampling section takes sine wave as analog input and samples the analog input at therate equal to the sampling signal.

For sample and hold circuit, the output is taken across a capacitor, which holds the level of the samples until the next sample arrives. For flat top sampling clock used is inverted to that of sample & hold circuit. Output of flat top sampling circuit is pulses with flat top and top corresponds to the levelof analog signal at the instant of rising edge of the clock signal.

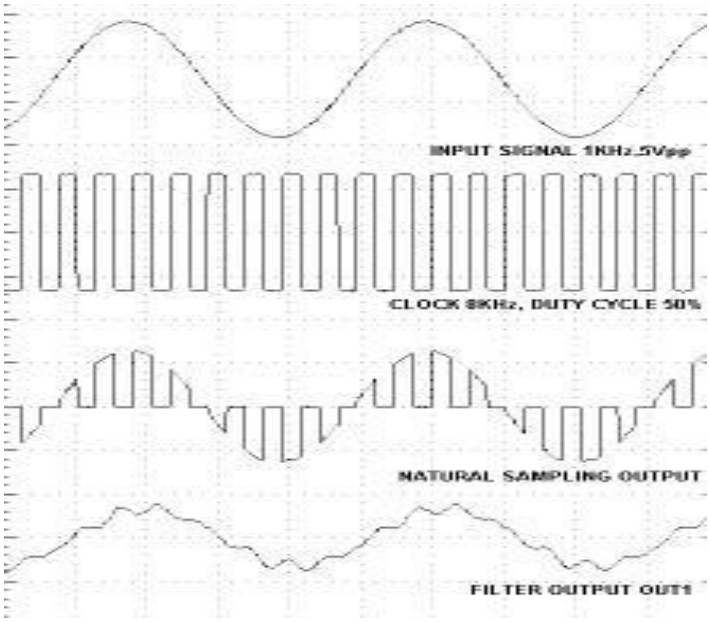
Filter Section

Two types of Filters are provided on board, viz., 2nd Order and 4th Order LowPass Butterworth Filter.

PROCEDURE

1. Refer to the Block Diagram & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on board, to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **(SW4)**.
5. Using clock selector switch **(S1)** select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Natural sampling block to the input **IN1** post of the 2nd Order LowPass Butterworth Filter and take necessary observation as mentioned below.
8. Repeat the procedure for the 2KHz sine wave signal as input.

MODEL WAVEFORMS



RESULT:

Exp. No. :4 **Date:**

DELTA MODULATION AND DEMODULATION

AIM

To verify delta modulation and demodulation.

EQUIPMENTS

- VCT-32
- Two channel 20MHz oscilloscope
- Function generator 1Hz - 100KHz
- Patch chords and probe

THEORY

Delta modulation process comes by quantizing the difference between analog information signal and integrated signal of one bit quantizer output, the integrator output is the approximation of analog input signal. The name delta modulation comes by taking difference between analog signal and integrator signal (DAC output).

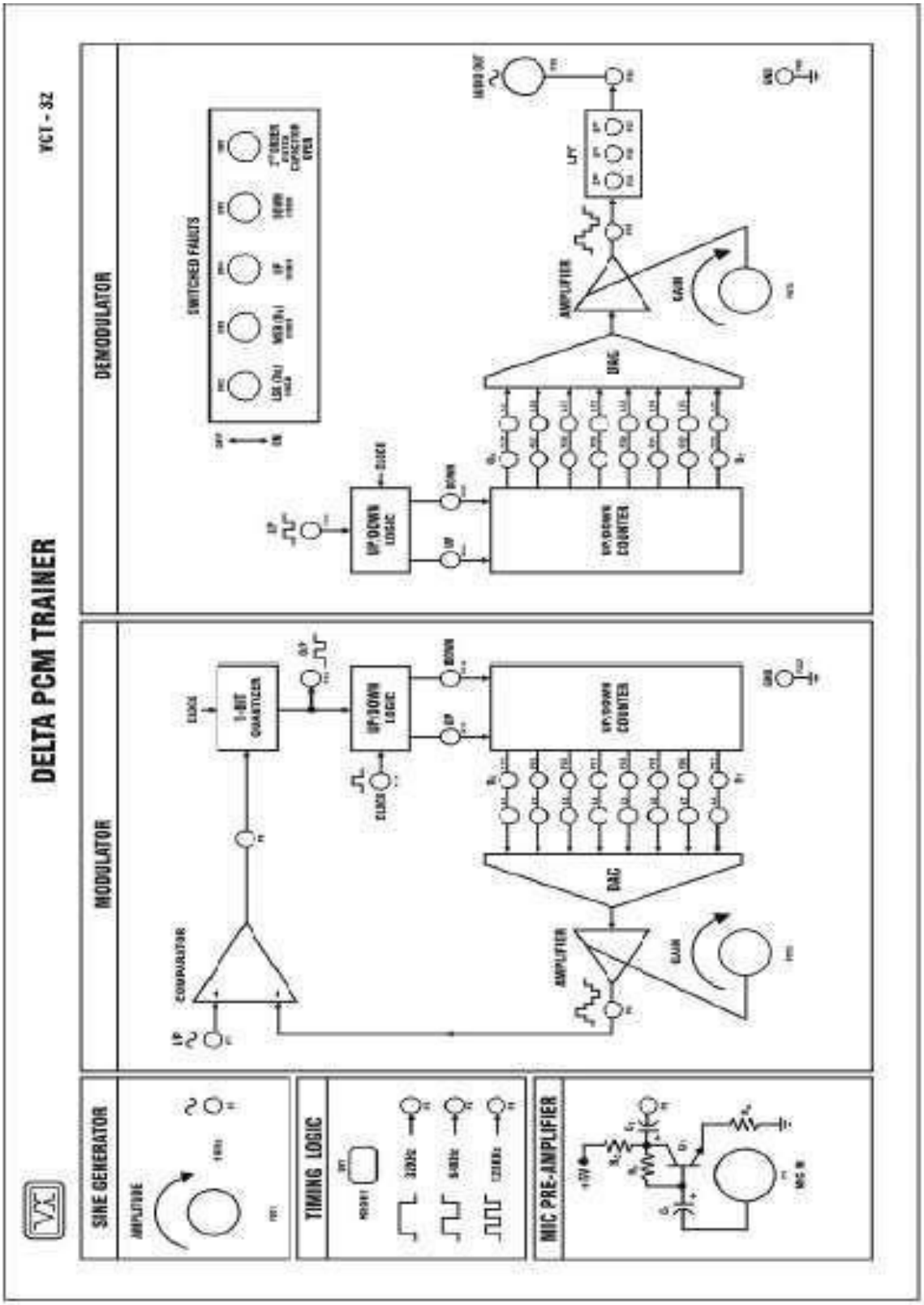
Front end of the modulator consists of a comparator which compares input analog signal x(t) with feedback (integral) signal i(t), when x(t)>i(t) output goes to high state and when x(t)<i(t) output goes to low state. The comparator output is then latched into a flip flop which is clocked by transmitter clock and so the data synchronized with the rising edge of the clock pulse. The DM output data is feed to the feedback loop of modulator which comprises 8-bit counter and Digital to Analog Converter(DAC). DAC output i(t) is an approximation of the input analog signal x(t).

The delta demodulator consist of only feedback section of modulator and a 6th order low pass filter to recover the analog information.

The trainer comes with an on-board 1KHz sinewave generator to be feed as a analog signal for the modulator, amplitude of 1KHz signal can be varied using POT 1.

Synchronized three clock pulses are provided (32KHz, 64KHz, 128KHz) to sample the modulator, students can select either one for the modulation purpose.

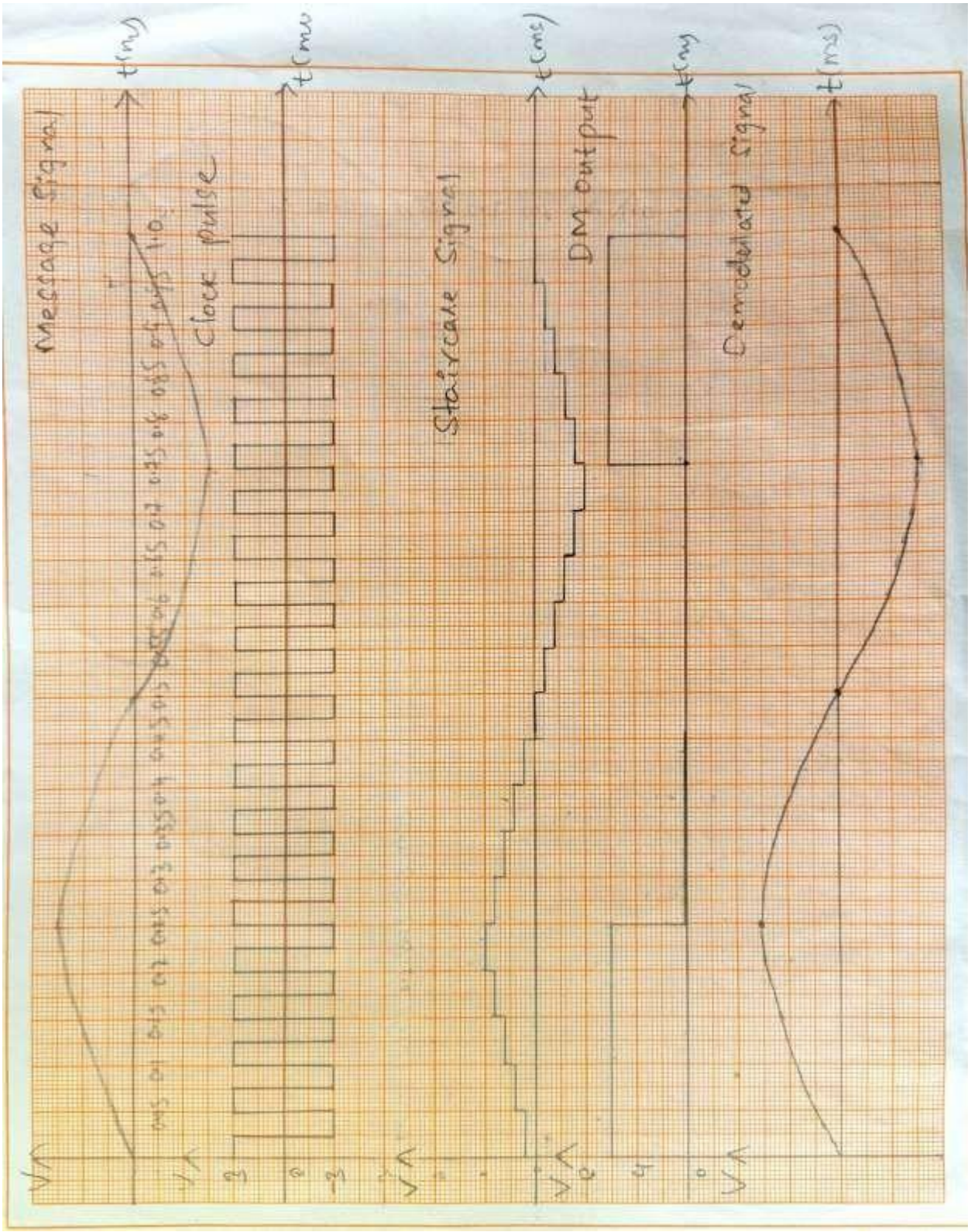
BLOCK DIAGRAM



PROCEDURE

1. Make wiring connection on VCT-32 as shown in figure 3.1 (or) simply connect the test points P1 to P7, P3 to P11 and P10 to P23 using patch chords provided with this training kit.
2. Ensure that all switches in switched faults block in OFF position and all potentiometers POT1, POT2 & POT3 in minimum position.
3. Display the modulating signal at test point P1 using a probe on channel 1 of oscilloscope. Increase sinewave amplitude by rotating POT 1 in clockwise direction and set sinewave amplitude to 3Vpp and note down.
4. Display the clock signal at test point P3 on channel 2 of oscilloscope and note down the waveform. Replace the channel2 by digital-to analog converter waveform (test point P8) and note down staircase waveform with respect to the modulating signal.
5. Now replace the channel 1 waveform by the delta modulated waveform (test point P10) and note down the modulated waveform with respect to the staircase signal.
6. Plot all the noted waveforms such as modulating signal, clock, staircase and modulated signal on a linear graph sheet.
7. Display the modulated waveform (P23) on channel 1 and demodulated staircase waveform (P34) on channel 2 of oscilloscope, increase gain control potentiometer POT 3 and set staircase signal amplitude to 3Vpp, note down waveforms.
8. Display the demodulated signal (test point P38) on channel 1 of oscilloscope and note down. Plot all the noted waveforms such as modulated signal, staircase waveform and demodulated signal on a linear graph sheet.

MODEL WAVEFORMS



RESULT:

Exp.No:5 **Date:**

AMPLITUDE SHIFT KEYING MODULATION AND DEMODULATION

AIM : To study the generation and detection of Amplitude ShiftKeying (ASK).

EQUIPMENTS :

APPARATUS	RANGE	QUANTITY
ASK modulation and demodulation trainer kit		1
Digital storage oscilloscope	100MHz	1
Power supply		1
Probes		As per req.
Patch cord		As per req.
Connecting wires		As per req.

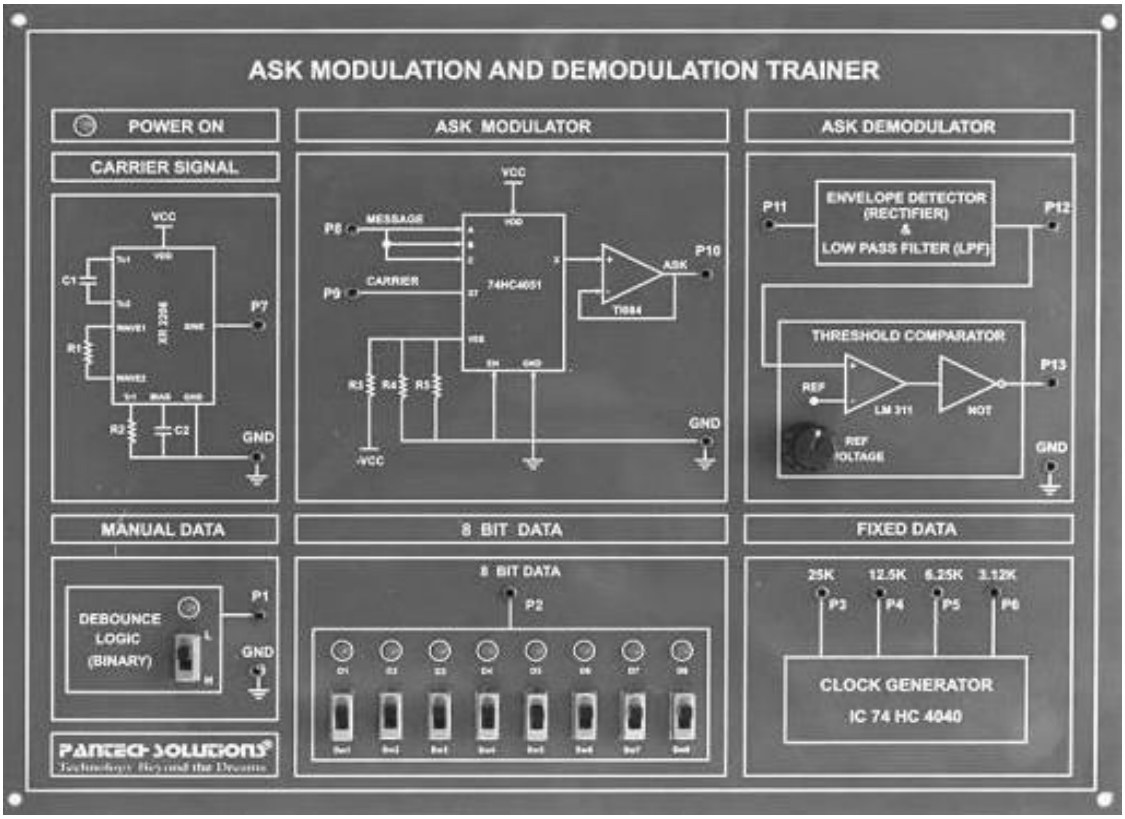
THEORY:

The binary ASK system was one of the earliest form of digital modulation used in wireless telegraphy. In a binary ASK system binary symbol 1 is represented by transmitting a sinusoidal carrier wave of fixed amplitude Ac and fixed frequency fc for the bit duration Tb whereas binary symbol 0 is represented by switching of the carrier for Tb seconds. This signal can be generated simply by turning the carrier of a sinusoidal oscillator ON and OFF for the prescribed periods indicated by the modulating pulse train. For this reason the scheme is also known as on-off shifttesting.

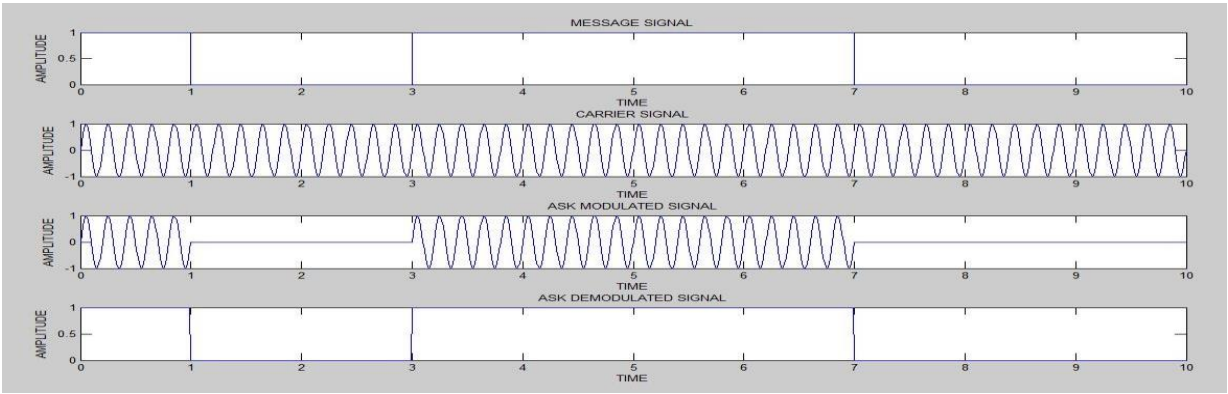
PROCEDURE:

1. The connections are given as per the block diagram.
2. Connect the power supply in proper polarity to the kit and & switch it on.
3. Set the amplitude and frequency of the carrier wave as desired.
4. Set the message data bit.
5. Observe the waveforms at the
    a. Message data
    b. Carrier signal
    c. ASK modulator output
    d. ASK demodulator output
6. Plot it on graph paper.

BLOCK DIAGRAM/ CIRCUIT DIAGRAM:



GRAPH:



OBSERVATION:

SIGNAL	AMPLITUDE(v)	TIME PERIOD	FREQUENCY
Message signal			
Carrier Signal			
ASK modulated signal			
Demodulated output			

RESULTS:

Exp. No.:6 **Date:**

FREQUENCY SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Frequency shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

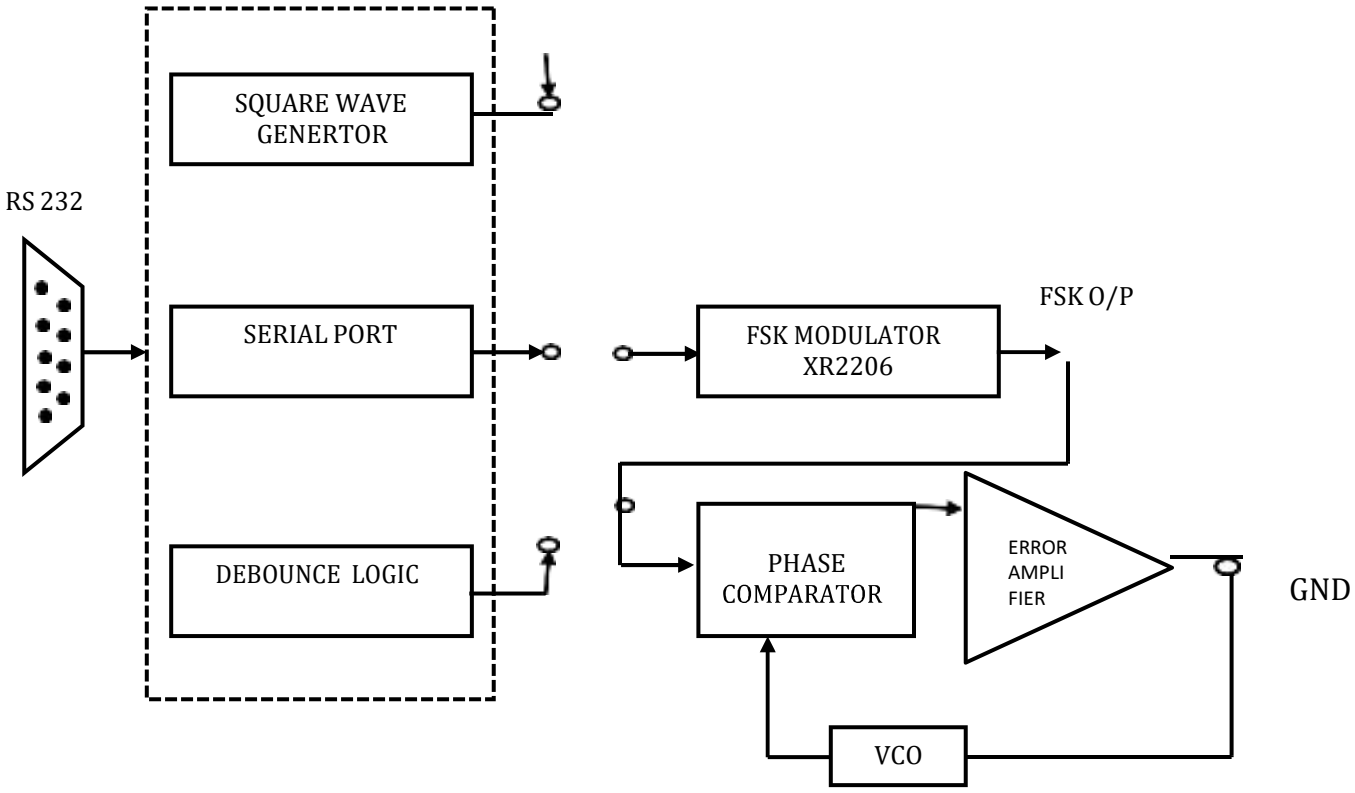
THEORY

Frequency-shift keying (FSK) is the frequency modulation system in which digital information is transmitted through the discrete frequency change of a carrier wave. The technology is used in communication systems such as amateur radio, caller ID, and urgent situation broadcasts. The simplest FSK is binary FSK (BFSK). BFSK uses a pair of discrete frequencies to transmit binary (0s and 1s) information. With this scheme, the "1" is called the mark frequency and the "0" is called the space frequency.

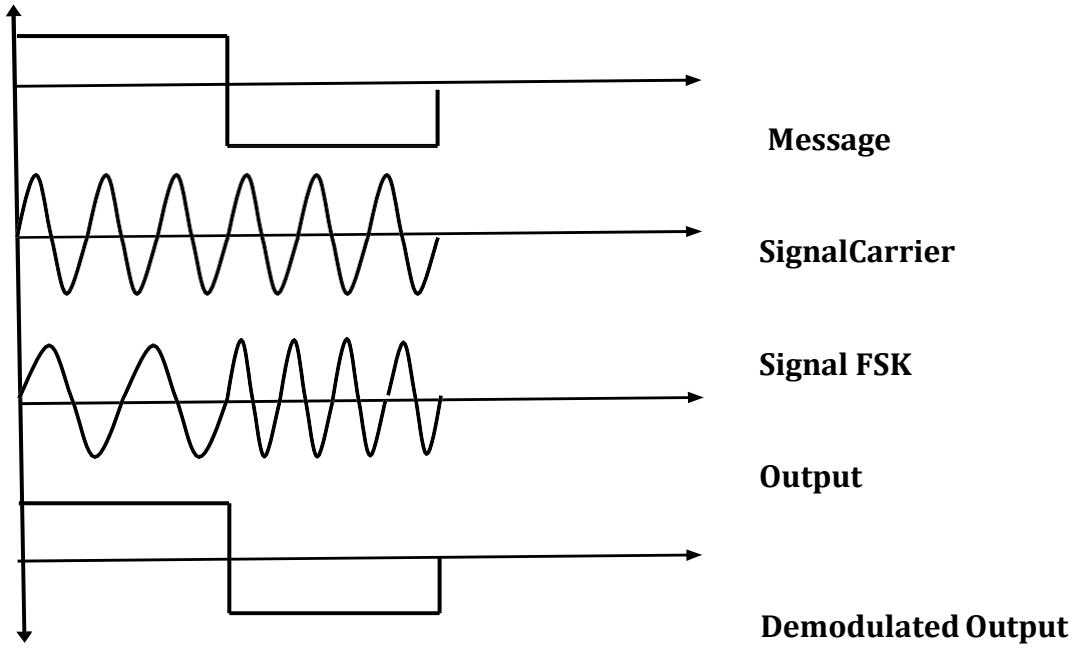
PROCEDURE

1. Switch on experimental kit.
2. Observe the message signal at the output of square wave generator
3. Observe the carrier signal at the output of FSK modulator without applying message.
4. Observe the FSK output at modulator by applying message.
5. Connect the FSK modulated output to the FSK demodulator and observe the output on CRO.

BLOCK DIAGRAM



MODEL WAVEFORMS



RESULT:

Exp. No.:7 **Date:**

PHASE SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

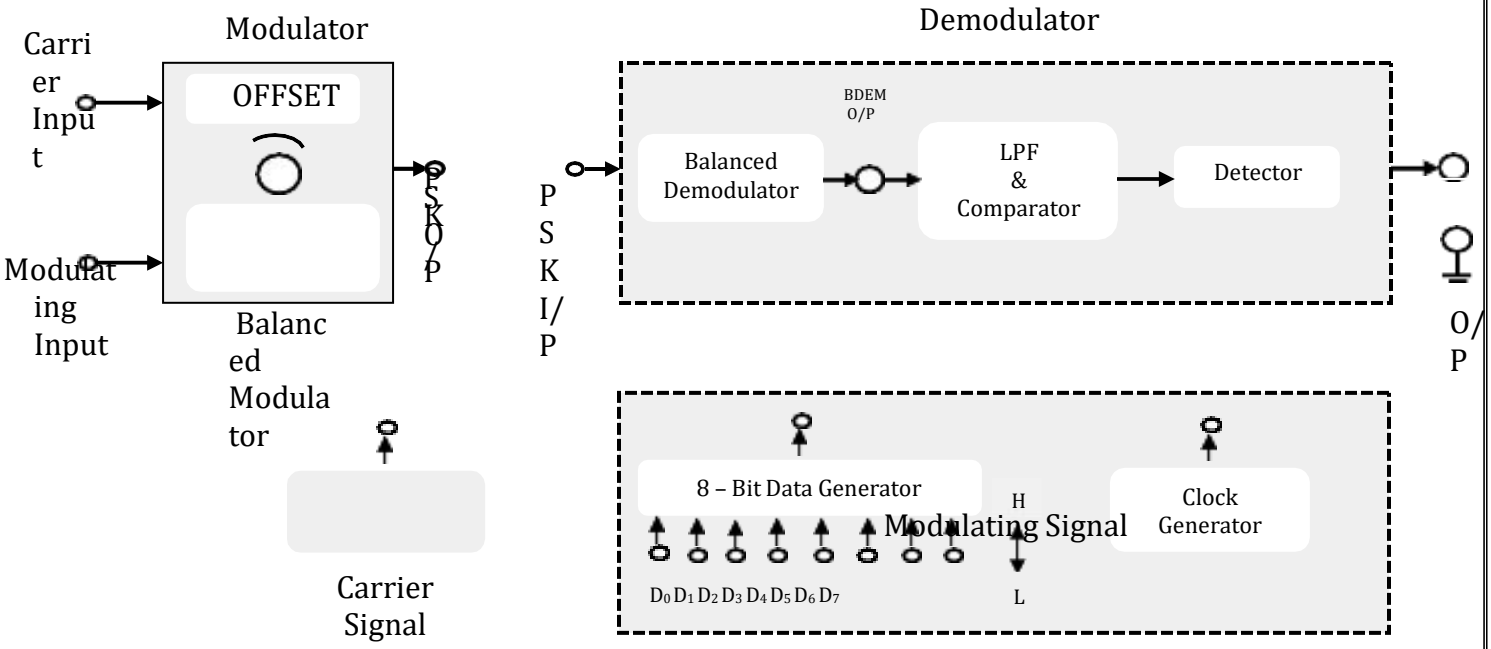
- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

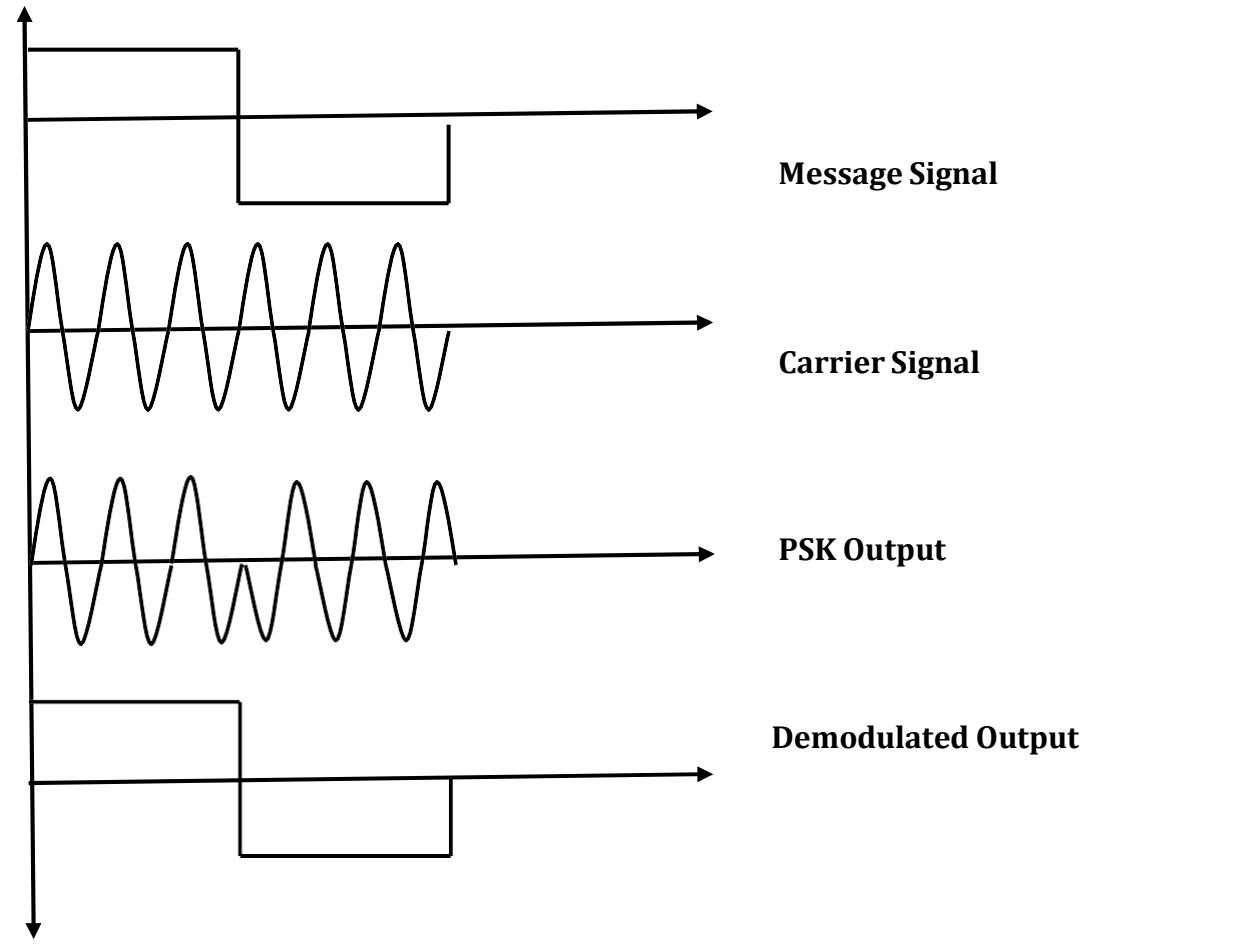
Phase shift keying (PSK) involves the phase shift change of the carrier sine wave between 0º and 180º in accordance with the data stream to be transmitted. PSK is also known as phase reversal keying (PRK).

Functionally, the PSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. Bit in contrast to ASK technique , the digital signal applied to the modulation input for PSK generation is bipolar i.e. have equal positive and negative voltage levels. When the modulating input is positive the output of modulator is a sine wave in phase with the carrier input, Whereas for the negative voltage levels, the output of modulator is a sine wave which is shifted out of phase 180º from the carrier input.

BLOCK DIAGRAM



MODEL WAVEFORMS



PROCEDURE

1. Connect carrier output of carrier generator to carrier input to modulator
2. Connect modulating signal output to modulating input of modulator
3. Switch on experimental kit.
4. Observe the PSK output at modulator and observe PSK output changes accordingly.
5. Connect the PSK modulated output to the PSK demodulator.
6. Connect the output of PSK demodulator to LPF and observe the output on CRO.

RESULT

Exp. No.:8 **Date:**

DIFFERENTIAL PHASE SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Differential Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

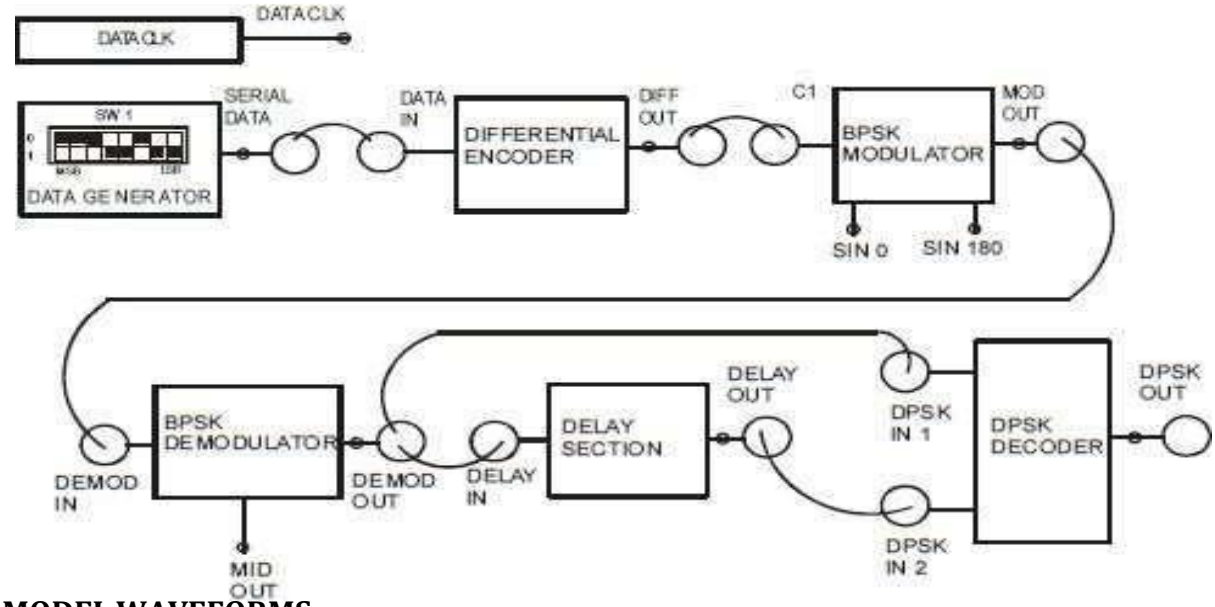
THEORY

In BPSK communication system, the demodulation is made by comparing the instant phase ofthe BPSK signal to an absolute reference phase locally generated in the receiver. The modulation is calledin this case BPSK absolute. The greatest difficulty of these systems lies in the need to keep the phase of the regenerated carrier always constant. This problem is solved with the PSK differential modulation, as the information is not contained in the absolute phase of the modulated carrier but inthe phase difference between two next modulation intervals.

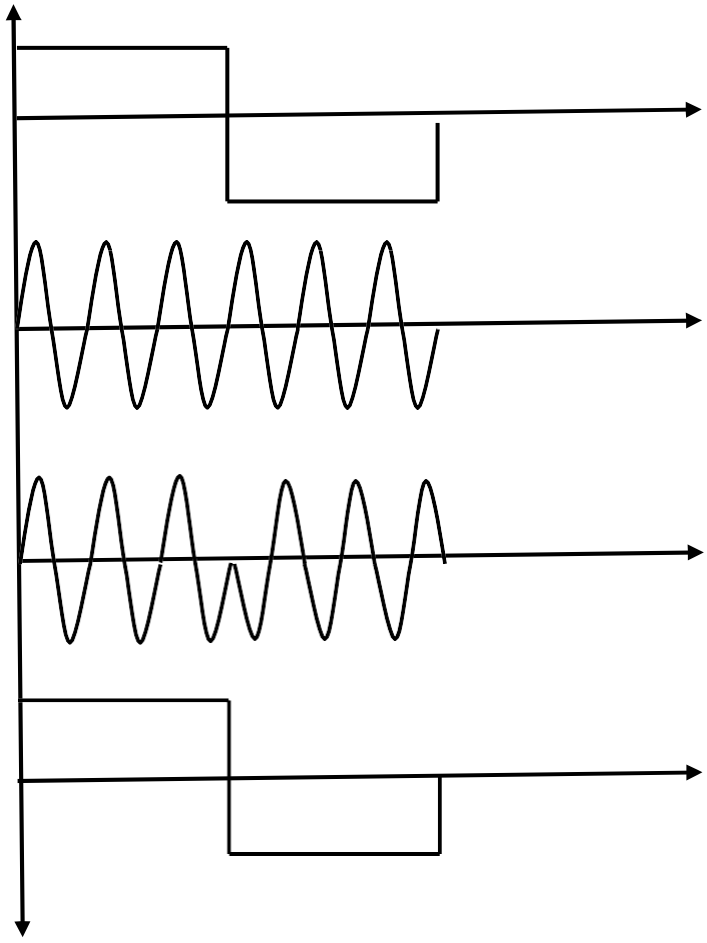
The coding is obtained by comparing the output of an EX-OR, delayed of a bit interval, with the current data bits. As total result of operation, the DPSK signal across the output of the modulator contains 180 deg. phase variation at each data bit "1". The demodulation is made by a normal BPSK demodulator, followed by a DPSK DECODER which is nothing but a decision device supplying a bit "1" each time there is a variation of the logic level across its input.

The DPSK system explained above has a clear advantage over the BPSK system in that the former avoids the need for complicated circuitry used to generate a local carrier at the receiver. To see the relative disadvantage of DPSK in comparison with PSK, consider that during some bit interval the received signal is so contaminated by noise that in a PSK system an error would be made in the determination of whether the transmitted bit was a 1 or 0. in DPSK a bit determination is made onthe basis of the signal received in two successive bit intervals. Hence noise in one bit interval may cause errors to two-bit determination. The error rate in DPSK is therefore greater than in PSK, and, asa matter of fact, there is a tendency for bit errors to occur in pairs. It is not inevitable however those errors occur in pairs. Single errors are stillpossible

BLOCK DIAGRAM



MODEL WAVEFORMS



Message Signal

Carrier Signal

DPSK Output

Demodulated Output

PROCEDURE

1. Refer to the block diagram and carry out the following connections.
2. Connect power supply in proper polarity to the kit DCL-DPSK and switch it on.
3. Select Data pattern of simulated data using switch SW1.
4. Connect the SERIAL DATA to the DATA IN of the DIFFERENTIAL ENCODER.
5. Connect differentially encoded data DIFF OUT of DIFFERENTIAL ENCODER to control inputC1 of BPSK MODULATOR.
6. Connect DPSK modulated signal MOD OUT of BPSK MODULATOR to DEMOD IN of the BPSKDEMODULATOR.
7. Connect DEMOD OUT of BPSK DEMODULATOR to DELAY IN of DELAY SECTION and one inputDPSK IN 1 of DPSK DECODER.
8. Connect the DELAY OUT of DELAY SECTION to the input DPSK IN 2 of DPSK DECODER.
9. Compare the DPSK decoded data at DPSK OUT with respect to input SERIAL DATA.
10. Observe various waveforms

RESULT

Exp. No.:9 **Date:**

QUADRATURE PHASE SHIFT KEYING - MODULATION AND DEMODULATION.

AIM

To verify Quadrature Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

In this modulation, called Quadrature PSK (QPSK) or 4 PSK the sine carrier takes 4 phase values, separated of 90 deg. and determined by the combinations of bit pair (Dibit) of the binary data signal. The data are coded into Dibit by a circuit generating:

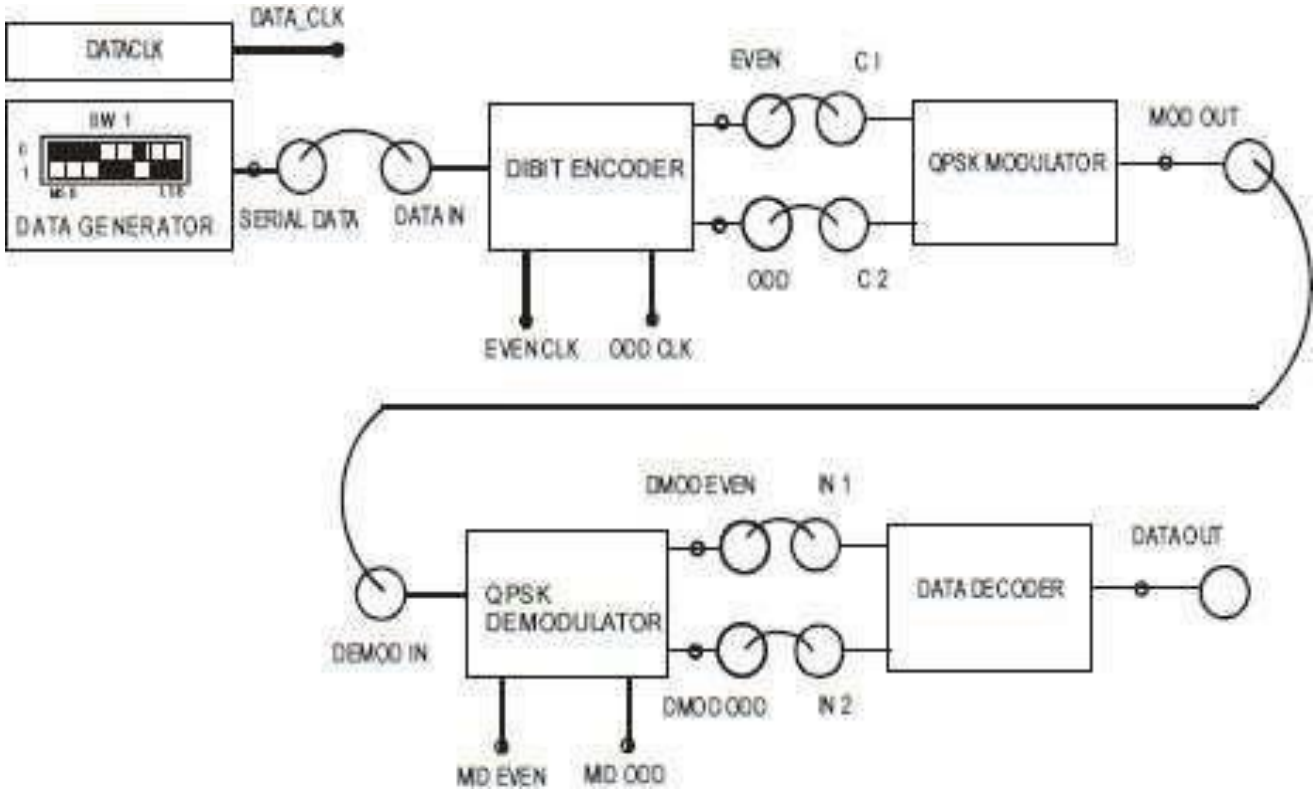
• A data signal **EVEN** (in phase) consisting in voltage levels corresponding to the value of thefirstbit of the considered pair, for duration equal to 2 bit intervals.

• A data signal **ODD** (in quadrature) consisting in voltage levels corresponding to the value ofthe second bit of the pair, for duration equal to 2 bit intervals.

The block diagram of the modulator used on the module is shown in the fig. four 1MHz sine carriers, shifted between them of 90 deg, are applied to modulator. The data (signal EVEN & ODD) reach the modulator from the Dibit Encoder. The instantaneous value of EVEN and ODD data bit generates a symbol. Since EVEN and ODD can take either 0 or 1 value, maximum 4 possible symbols can be generated (00, 01, 10, and 11). According to the symbol generated oneof the foursine carrier will be selected. The relation between the symbol generated and sine carrier is shown in table.

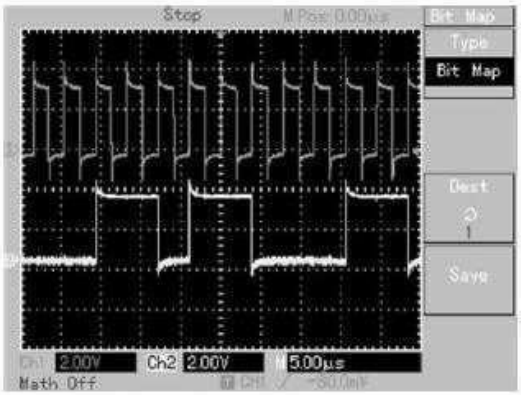
DIBIT		PHASE SHIFT
EVEN	ODD	
0	0	180 deg
0	1	90 deg
1	0	270 deg
1	1	0 deg

BLOCK DIAGRAM



MODEL WAVEFORMS

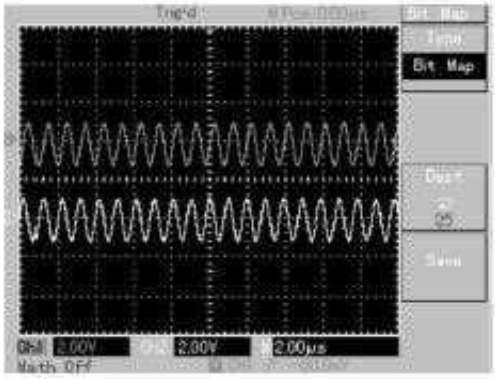
CH 1 : DATA CLK (256 KHz) & CH 2 : SERIAL DATA (00011011)



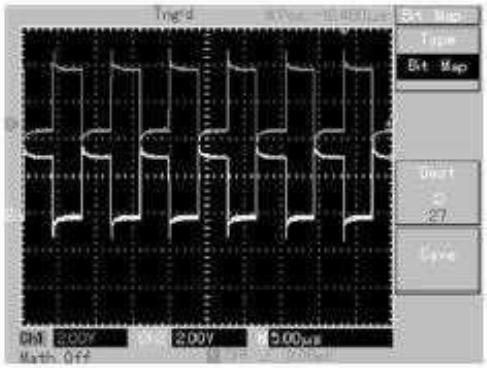
A receiver for the QPSK signal is shown in fig. synchronous detection is required and hence it is necessary to locally regenerate the carriers. The scheme for carrier regeneration is similar to that employed in BPSK. In that earlier case we squared the incoming signal to remove the phasedifference, and recovered the data by filtering. The incoming signal is applied to the multipliers to remove the phase shift.

The output of the multipliers can be seen at MID EVEN and MID ODD posts. The output of the multipliers is then given to filters, where we get the recovered even and odd data at the DEMOD EVEN and DEMOD ODD posts. These recovered EVEN & ODD bits having exactly same phase & frequency compared to transmitter EVEN & ODD bit. These EVEN & ODD bits then applied to DATA DECODER logic to recover the original NRZ-L data pattern.

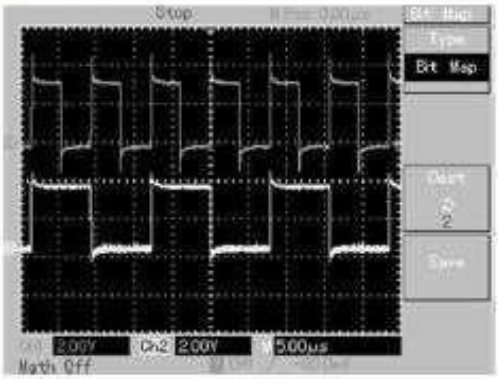
CH 1: SIN 180 (1 MHz) & CH 2: SIN 270 (1 MHz)



CH 1 : EVEN CLK (128 KHz) & CH 2 : ODD CLK (128 KHz)



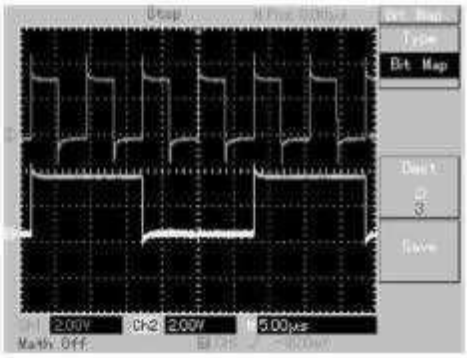
CH 1 : EVEN CLK (128 KHz) & CH 2 : EVEN DATA



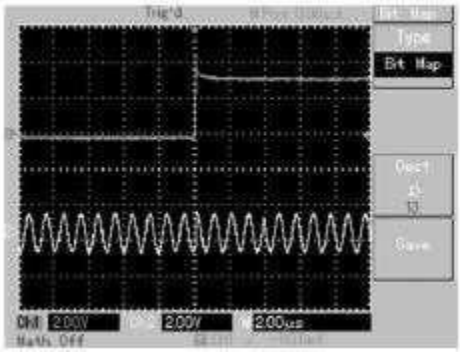
PROCEDURE

2. Refer to the block diagram and carry out the following connections and switch settings.
3. Connect power supply in proper polarity to the kits DCL-QPSK and switch it on.
4. Select Data pattern of simulated data using switch SW1.
5. Connect SERIAL DATA generated to DATA IN of the DIBIT ENCODER.
6. Connect the dibit data EVEN & ODD bit to control input C1 and C2 of QPSK MODULATORrespectively
7. Connect QPSK modulated signal MOD OUT to the DEMOD IN of the QPSK DEMODULATOR.
8. Connect DEMOD EVEN & DEMOD ODD outputs of QPSK DEMODULATOR to IN 1, & IN 2posts of Data Decoder respectively.
9. Observe various waveforms as mentioned below

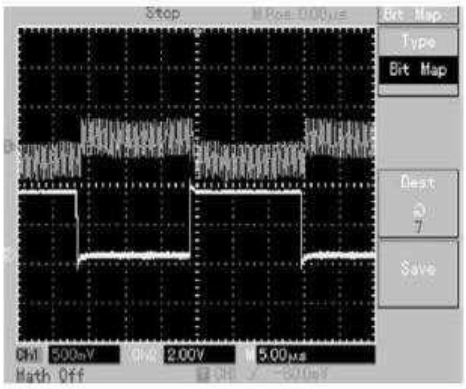
CH 1 : ODD CLK (128 KHz) & CH 2 : ODD DATA



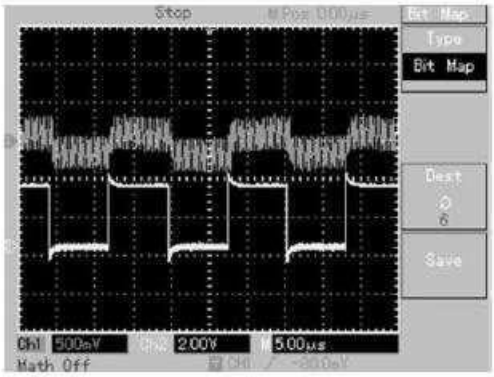
CH 1 : EVEN & CH 2 : MOD OUT



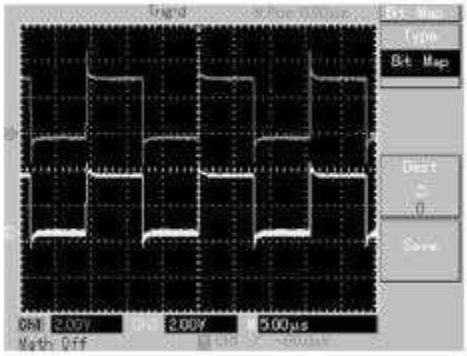
CH 1 : MID ODD & CH 2 : DEMOD ODD



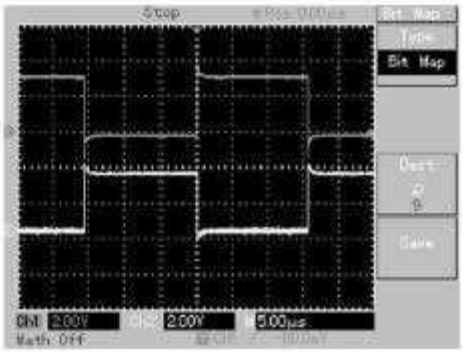
CH 1 :MID EVEN & CH 2 : DEMOD EVEN



CH 1 : EVEN & CH 2 : DEMOD EVEN



CH 1 :ODD & CH 2 : DEMOD ODD



RESULT:

Exp. No.: 10 **Date:**

BINARY PHASE SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Binary Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

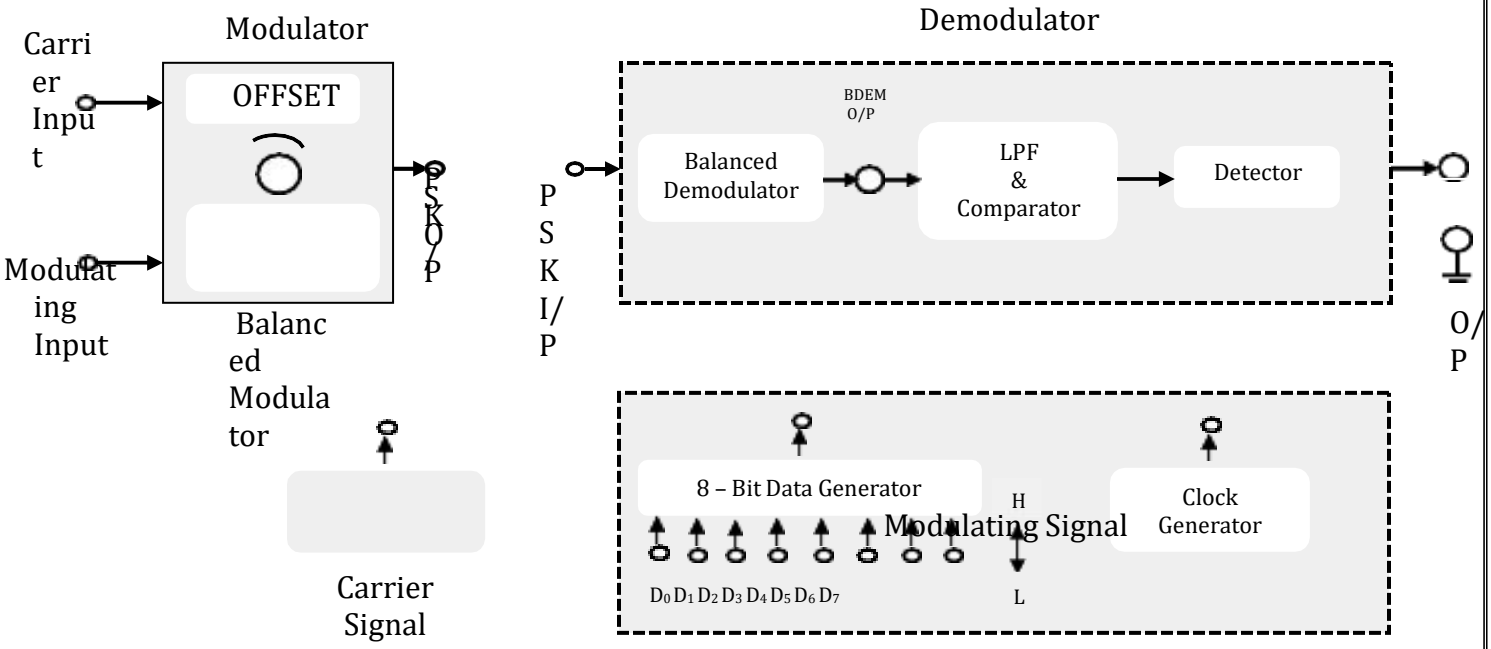
- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

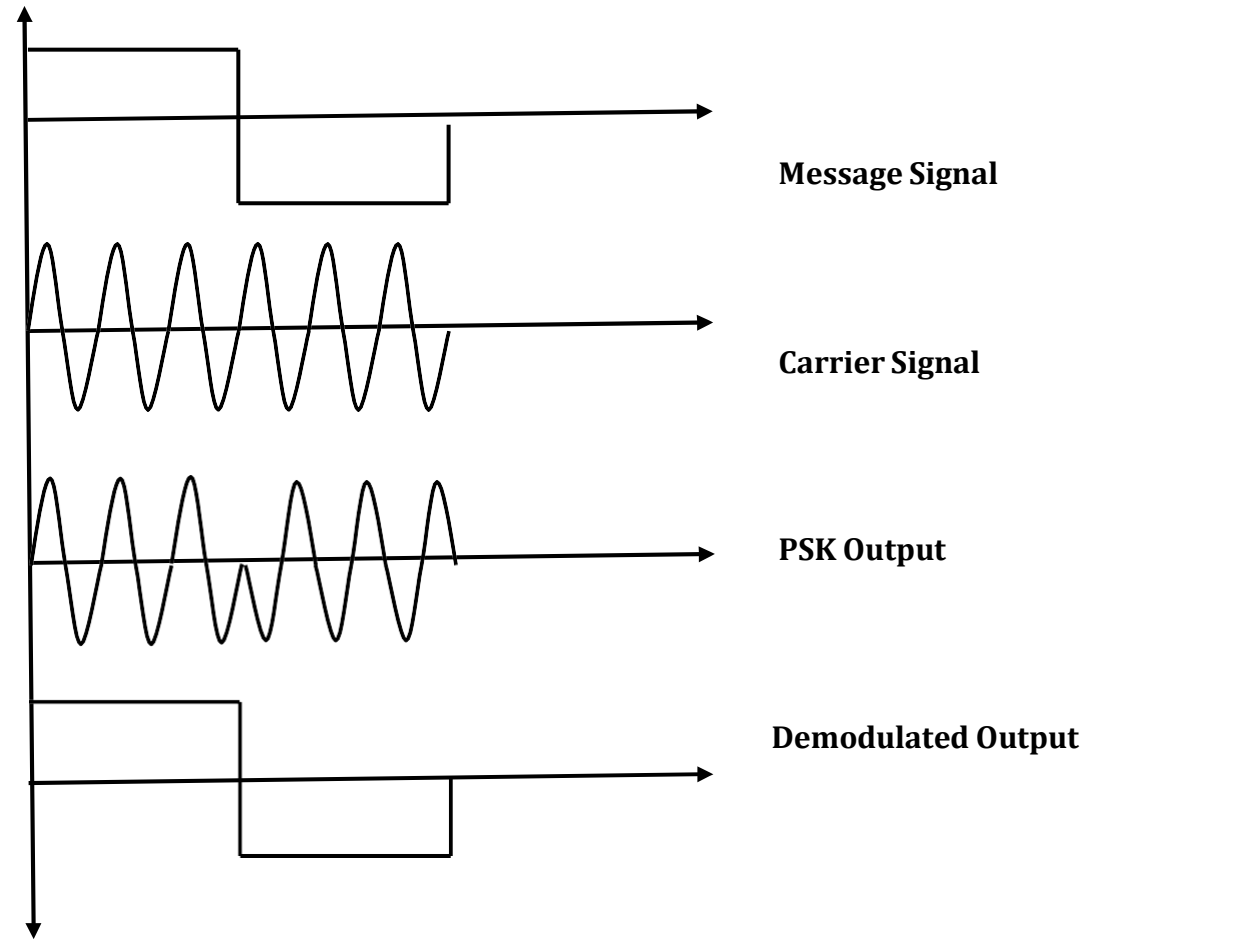
Binary Phase shift keying (BPSK) involves the phase shift change of the carrier sine wave between 0º and180º in accordance with the data stream to be transmitted. BPSK is also known as Binary Phase Reversal Keying (BPRK).

Functionally, the BPSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. Bit in contrast to ASK technique , the digital signal applied to the modulation input for BPSK generation is bipolar i.e. have equal positive and negative voltage levels. When the modulating input is positive the output of modulator is a sine wave in phase with the carrier input, Where as for the negative voltage levels, the output of modulator is a sine wave which is shifted out of phase 180º from the carrier input.

BLOCK DIAGRAM



MODEL WAVEFORMS



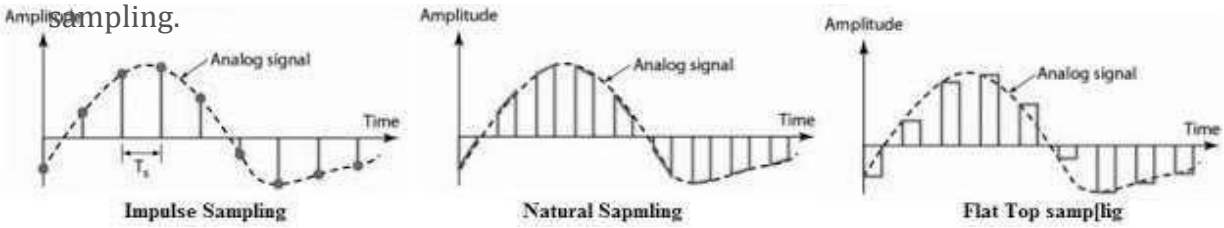
PROCEDURE

7. Connect carrier output of carrier generator to carrier input to modulator
8. Connect modulating signal output to modulating input of modulator
9. Switch on experimental kit.
10. Observe the BPSK output at modulator and observe BPSK output changes accordingly.
11. Connect the BPSK modulated output to the BPSK demodulator.
12. Connect the output of BPSK demodulator to LPF and observe the output on CRO.

RESULT:

VIVA QUESTIONS AND ANSWERS:

1. **What are the disadvantages of Analog communication?**
   Its not reliable, Noise effect is more on the signals, Power required forsignaltransmission also more, Circuit complexity is more and costly.
2. **What are the Advantages of Digital Communication?**
   Reliable, Noise effect is very less, power consumption is very less, various Digital ICs areavailable so circuits not complex , cheap, Error detection and correction is also possible.
3. **What are different types of digital modulation?**
   ASK, FSK, PSK, PCM, DPCM,Delta modulation, Adaptive Delta modulation etc..
4. **How to convert an analog signal into digital signal?**
   Blocks: Anti aliasing filter, Sampler, Quantizer, encoder.
5. **Define the functionality of Sampler, Quantizer?**
   Sampler: converts a continuous time signal into discrete time signal.
   Quantizer: converts continuous in amplitude signal into discrete in amplitude signal.
6. **What are some Coding techniques?**
   Pulse code modulation, Differential pulse code modulation, Delta modulation, Adaptive deltamodulation.
7. **What is Sampling?**
   Converting a continuous time signal into discrete in time signal is called as Sampling (similartocutting a bread into slices)
8. **Define Sampling theorem?**
   To reconstruct the Continuous time signal from discrete time signal ,the sampling frequencyshould be more than equal to twice of Continuous time signal frequency(max).
9. **What is Nyquist Rate?**
   If the sampling frequency is twice of Continuous time signal frequency(max), then thatiscalled as Nyquist rate.
10. **How many types of samplings are their? Explain briefly?**Impulse Sampling, Natural sampling, Flat top sampling.



11. **What is aliasing effect? How to overcome it?**
    Due to imperfect sampling the signals will be interfered in frequency domain i.e calledaliasing effect in sampling. if sampling theorem satisfied in sampling or first by passingsignal from anti aliasing filter before sampling then aliasing effect will be reduced
12. **What are the Analog pulse modulation methods?**
    Pulse amplitude modulation, pulse width modulation and pulse position modulation..
13. **Define Pulse amplitude modulation?**
    The carrier pulse height (amplitude) proportional to amplitude of messege signal.
14. **Define Pulse width modulation?**
    The carrier pulse width proportional to amplitude of message signal.

15. Define Pulse position modulation?

The carrier pulse position proportional to amplitude of message signal.

16. Compare PAM, PWM, PPM?

	PAM	PWM	PPM
Pulse amplitude	variable	constant	constant
Pulse width	constant	variable	constant
Pulse position	constant	constant	variable
Bandwidth	less	High	High
Power required	Low	Moderate	Highest
Complexity	Low	Moderate	Highest

17. What is Amplitude shift Keying (ASK) ?

It represent the digital data as variations in amplitudes in carrier wave. i.e '1' represented bytransmitting a fixed amplitude carrier wave for the bit duration with constant frequency.

18. What is Phase shift keying (PSK)?

It represent the digital data as variations in phase shift in carrier wave. i.e '1' represented by 0phase shift carrier wave , where '0' represented as 180 phase shift incarrier wave for the bit duration with constant frequency

19. What is Frequency shift keying (FSK) ?

It represent the digital data as variation in frequency in carrier wave, i.e for '1' morethancarrier frequency , for '0' less than carrier frequency.

20. What is Binary Phase shift Keying (BPSK) ?

for each one bit of binary data (0 & 1) carrier phase will be changed (two different shifts: 0,180)

21. What is Quadrature Phase shift Keying (QPSK) ?

for each two bits of binary data (00,01,10 & 11) carrier phase will be changed (four differentshifts : 45, 135, -45, -135)

22. What is the difference between Bit Rate and Baud Rate?

Bit rate represents Bits per sec,Baud rate represents no. of symbols per second i.e. in communications the no. of bits transmitted per sec is called as Bit Rate (units bps) and Theno. of times a signal (here carrier) changes its state (change in freq, phase, amplitude) per secis called as Baud rate.

23. What is bandwidth of BPSK signal?

2Fc, if Fc represents carrier frequency

24. Compare ASK, PSK and FSK.? Bandwidth: ASK< PSK < FSK Power: ASK <PSK = FSK

Probability of error: ASK > PSK > FSK

Signal toNoise Ratio: ASK < PSK < FSK

25. Why is ASK called as ON-OFF keying?

When input data is 1 then output is carrier, if input is 0 out put is zero. so its looks likea switch which will switch on when input is 1 and off when input is zero.

26. Define Pulse code modulation?

Each and every quantized samples will be encoded with sequence of zeros and ones with 'n'

bits within sampling interval (Ts), So the bit duration will be Ts/n. as no. of bits (n) increaseserror decreases but bandwidth increases.

27. How bits are needed to encode N different levels?$Log_2 N$

28. Define step size?

It is the difference between two successive no.s (levels), i.e. voltage difference between onedigital level and the next digital level. (Ex: 000 & 001, 1011 & 1100)

29. How to calculate Step size in PCM?step size(Δ) = $(V_{FS}-V_{min})/L$

where $L = 2^n$, n = no. of bits, VFS = full scale voltage

30. Define Quantization error?

It is the difference between sampled signal and Quantized signal.

31. What is the max value of Quantization error?Half of the Step size.

32. What are the applications of PCM?

computer Disk, Digital Telephony, Digital Audio Applications, etc.

33. What are the disadvantages of Pulse code modulation?

To get less Quantization Noise no. of bits should be increased, then bandwidth willbeincreased. So we have to compromise with either Quantization error or bandwidth.

34. Define Differential pulse code modulation?

In DPCM, The difference between the consequent samples will be encoded with sequenceofzeros and ones.

35. Why DPCM is better than PCM?

Instead of encoding each sample, Its better to encode the difference between samples thenQuantization error will be minimized with less no. of bits, then bandwidth also get decreased.

36. Define Delta modulation? Why it is better?

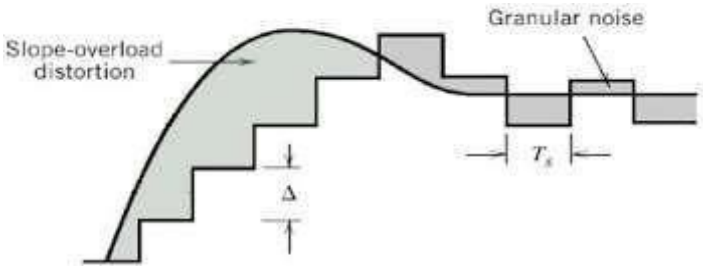
It is same as DPCM with no. of bits to encode is one bit only (either 0 or 1). by this bandwidth will be decreased.

37. What is granular noise? Define slope overload?

The Delta modulation is efficient when and only when signal is varying continuously withless variations. if signal varies suddenly then we get two different Noises. those are slopeoverload and granular noise

38. When granular noise and slope overload occur in Delta modulation?Granular Noise: $\Delta / T_s >$ slope of signal

Slope Overload Noise: $\Delta / T_s <$ slope of signal



39. What is Adaptive Delta Modulation and what are the advantages?

If the step size varies according to the slope of the signal then that is called as Adaptive Deltamodulation. granular and slope over load noise will be desuced.

40. Compare all Digital pulse modulation techniques (PCM, DPCM, DM, ADM)?

	PCM	DPCM	DM	ADM
No. of bits needed	more	less	1	1
Bit duration	very less	less	T_s	T_s
Bandwidth	very high	high	$1/T_s$	$1/T_s$
Circuit complexity	high	high	less	less
Step size	very less	less	high	varies
Quantization error	high	less	less	less

41. What is multiplexing? How many types of multiplexing possible in communication? Combining two or more signals to pass through a channel is called as multiplexing. The different Multiplexing techniques are:1) Frequency division Multiplexing, 2) Timedivision Multiplexing, 3) Wavelength division multiplexing, 4) Orthogonal frequency division multiplexing.

42. What is Line coding and what are the different line coding techniques?

Line coding is the representation of digital data (0,1) as puses. the types in line coding are:Non Return to Zero (NRZ), Return to Zero (RZ), Biphase, Differential Manchester, Bipolar

43. What is the difference between Source coding and Line coding?

Source Coding is used to represent analog signals in form of Digital data (like PCM,DPCM,DM), where Line Coding is used to represent digital data in the form of pulses(like NRZ, RZ)

44. Define ISI (Inter symbol Interference)?

It is a Distortion in digital signal that one symbol interferes with other symbol.

45. What is Matched filter?

It is an optimal linear filter for maximizing the SNR (Signal to Noise Ratio) in the presenceof additive random noise.

46. What is the cause of inter symbol Interference (ISI) and it can be reduced?

ISI caused by multipath propagation and inherent non linear frequency response of channel.Itcan be reduced by pulse shaping.

47.What is multipath Interference?

When a signal reaches to transmitter in various paths then delays exist in each path so

at receiver all delayed signals will be received, then original signal will be interfered by itsdelayed versions. That is called multipath interference.

51. What is frequency synthesizer?

it is an oscillator which can generate any range of frequencies.Applications of frequency synthesizer?

52. Define polar encoding?

It is a line code of RZ (Return to Zero) in which binary 1 represented by +ve voltage and 0represented by zero volts.

53. Define bipolar encoding?

It is a line code of NRZ (Non Return to Zero) in which two non zero values are for encodingbinary data.

54. Define Manchester encoding?

It is a line code which will generated based on clock and binary data. The code is XOR logicofclock and digital data.

55. What are the features of Code Division Multiple Access?

The CDMA technique is more secure communication over all, this is used in military, If we know the code which is used to encode the data, then only we can receive the data. But No. ofusers are limited (depends on code length)

56. Explain about Frequency Division Multiple Access?

In FDMA Spectrum is divided into segments and each segment is permanently assigned to each transmitter. so to get more efficiency in using spectrum, each signal bandwidth shouldbe less and perfect modulation technique should be used.

57. Explain about Time division Multiple Access?

In this a fraction of time slot will be assigned to each transmitter, so as no. of transmitters increases complexity increases. for this perfect synchronization is required.