Sri Venkateswara College of Engineering and Technology, Chittoor. (Autonomous)

Department of Electronics and Communication Engineering

PULSE AND DIGITAL CIRCUITS LAB MANUAL (14AEC16)

(II B.Tech-II Semester ECE)

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PULSE & DIGITAL CIRCUITS LAB - 14AEC16

Objectives:

To familiarize student with

1. Generation and processing of sinusoidal and non-sinusoidal signals.
2. Fundamentals of basic logic gates and its applications.
3. Analysis and design of various multivibrator circuits.
4. Design and analysis of UJT relaxation oscillator and boot-strap sweep circuits

Outcomes:

After the completion of the lab, the student

1. Will be able to Generate and process sinusoidal and non-sinusoidal signals.
2. Will be able to understand fundamentals of basic logic gates and design applications.
3. Will be able to design and analyze various multivibrator circuits.
4. Will be able to design and analyze UJT relaxation oscillator and boot-strap sweep circuits

Minimum Twelve experiments to be conducted:

1. Linear wave shaping (RC Integrator & RC differentiator).
2. Non Linear wave shaping – Clippers.
3. Non Linear wave shaping – Clampers.
4. Transistor as a switch.
5. Study of Logic Gates & Some applications.
6. Half adder & Full adder.
7. Sampling Gates.
8. Astable Multivibrator.
9. Monostable Multivibrator.
10. Bistable Multivibrator.
11. Schmitt Trigger.
12. UJT Relaxation Oscillator.
13. Bootstrap sweep circuit.
14. Constant Current Sweep Generator using BJT.

Equipment required for Laboratories:

1. RPS: (0 – 30) V
2. CRO: (0 – 20) MHz
3. Function Generators :(0 – 3) MHz
4. Components
5. Multi Meters

INDEX

S No	Date	Name of the Experiment	Remarks

Exp No: 1 **Date:**

LINEAR WAVE SHAPING

(RC INTEGRATOR & RC DIFFERENTIATOR)

AIM:

i) To design and verify an integrator (Low pass RC) circuit.
ii) To design and verify a differentiator (High pass RC) circuit.

COMPONENTS REQUIRED:

1. Resistors 1kΩ, 10kΩ, 100kΩ
2. Capacitor 0.1 μf (1No.)
3. Bread Board
4. Connecting wires
5. CRO & Probes
6. Function Generator

THEORY: The process in which non sinusoidal signal is altered by transmission through a linear network is called "Linear wave shaping".

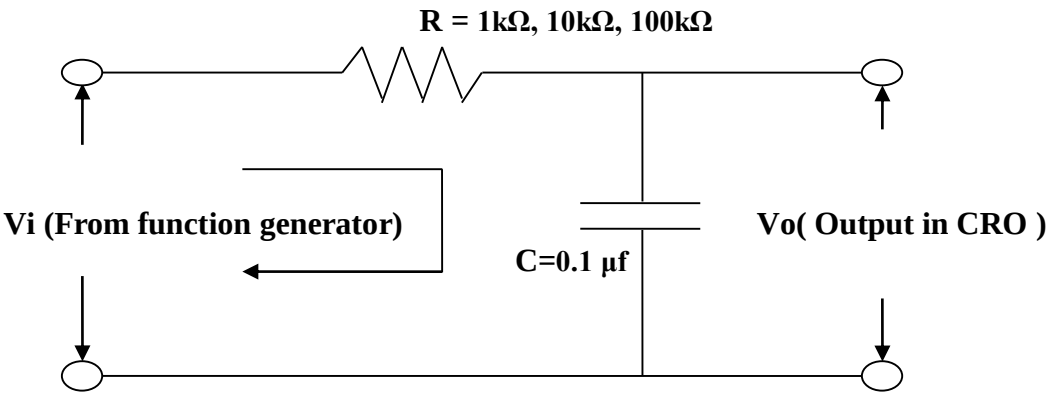
i) **RC INTEGRATOR (or) LOW PASS FILTER:** A Low pass circuit is a circuit which transmits only low frequency signals and alternates (or) stops high frequency signals at zero frequency, the reactance of the capacitor is infinity (i.e. the capacitor acts as a open circuit). So the entire input appears at the output i.e. the input is transmitted to the output with zero alternation. So the entire output is same as the input i.e. the gain is unity. As the frequency increase the capacitor reactance $X_C = 1/2\pi fc$ decreases and so the output decreases. At high frequencies the capacitor virtually acts as a short circuit and the output falls to zero. RC Integrator can be operated in three different modes i.e. Large Time constant$(RC \gg T)$, Medium Time constant $(RC = T)$ & Short Time constant $(RC \ll T)$.

ii) **RC DIFFERENTIATOR (or) HIGH PASS FILTER:** In a high pass RC circuit, at zero frequency the reactance of the capacitor is infinity and so it blocks the input and hence the output is zero. Hence this capacitor is called the blocking capacitor and this circuit also called the capacitive coupling circuit, is used to provide DC isolation between the input and output. As the frequency increases the reactance of the capacitor decreases and hence the output and gain increases. At very high frequencies the capacitive reactance is very small so a very small voltage appears across capacitor and so the output is almost equal to the input and the gain is equal to unity. Since this circuit attenuates low frequency signals and allows transmission of high frequency signals with

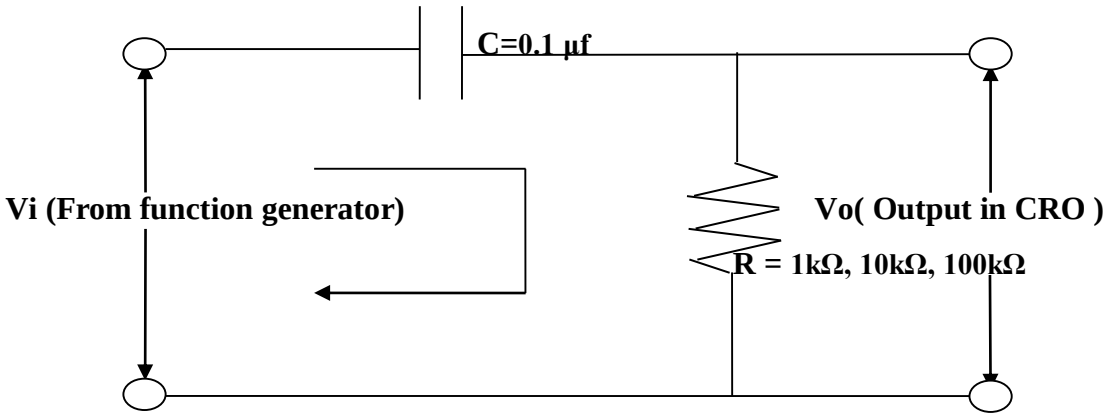
little or no attenuation, it is called a high pass circuit. RC differentiator can be operated in three different modes i.e. Large Time constant($RC \gg T$), Medium Time constant ($RC = T$) & Short Time constant ($RC \ll T$).

CIRCUIT DIAGRAM:

i) RC INTEGRATOR (or) LOW PASS FILTER:



ii) RC DIFFERENTIATOR (or) HIGH PASS FILTER:

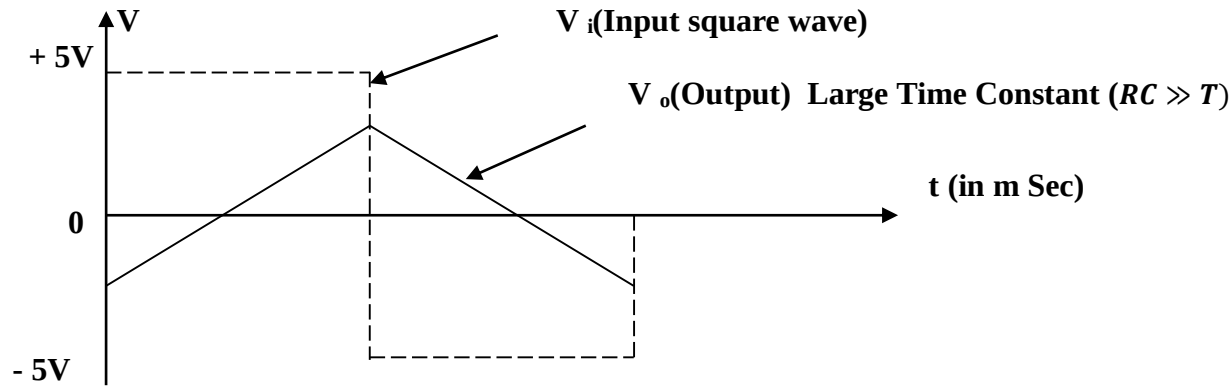


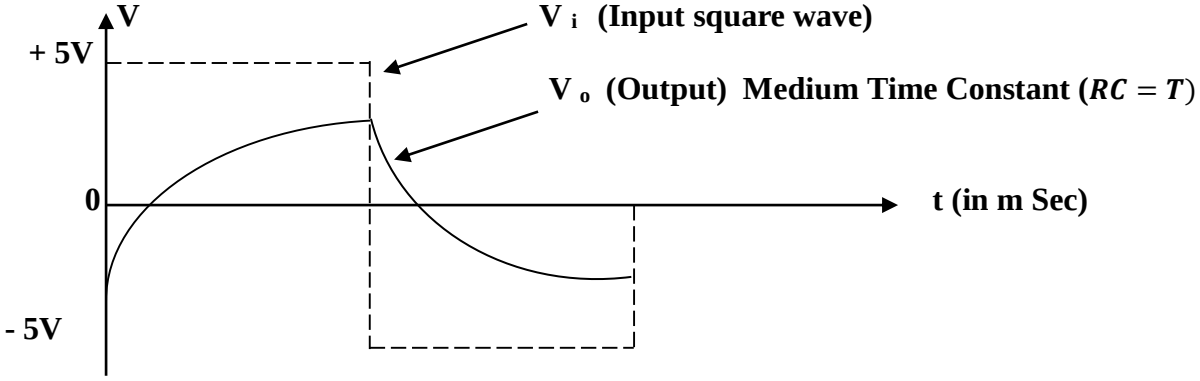
PROCEDURE:

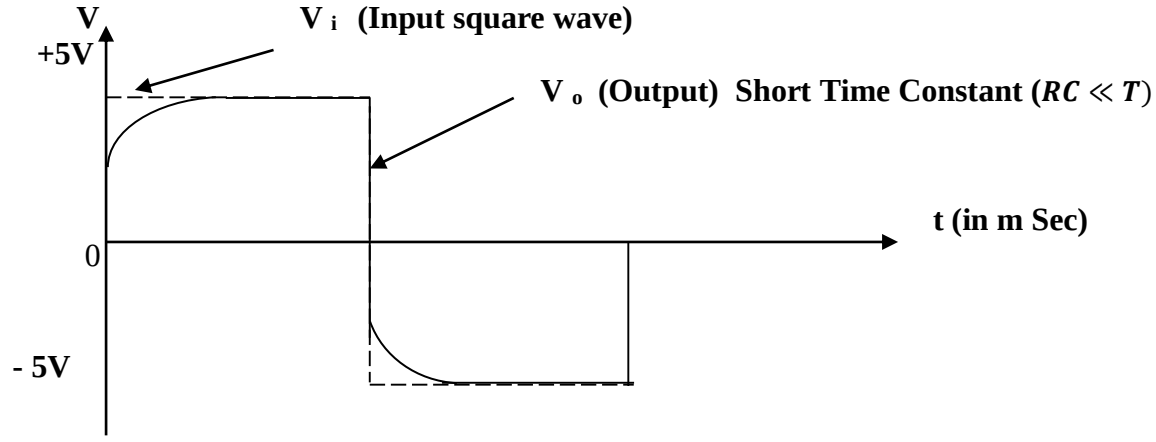
1. Connect the low pass circuit as per the circuit diagram.
2. Connect the function generator at the input terminals and CRO at the output terminals.
3. Apply a square wave signal of 10V amplitude and 1 KHz frequency at input.
4. Observe the output waveform of the circuit for different time constants.
   Large Time constant($RC \gg T$), Medium Time constant($RC = T$),Short Time constant($RC \ll T$).
5. Repeat the above procedure for high pass circuit also.
6. Draw the graph for both low pass and high pass circuits for above three cases of time constants.

MODEL GRAPH:

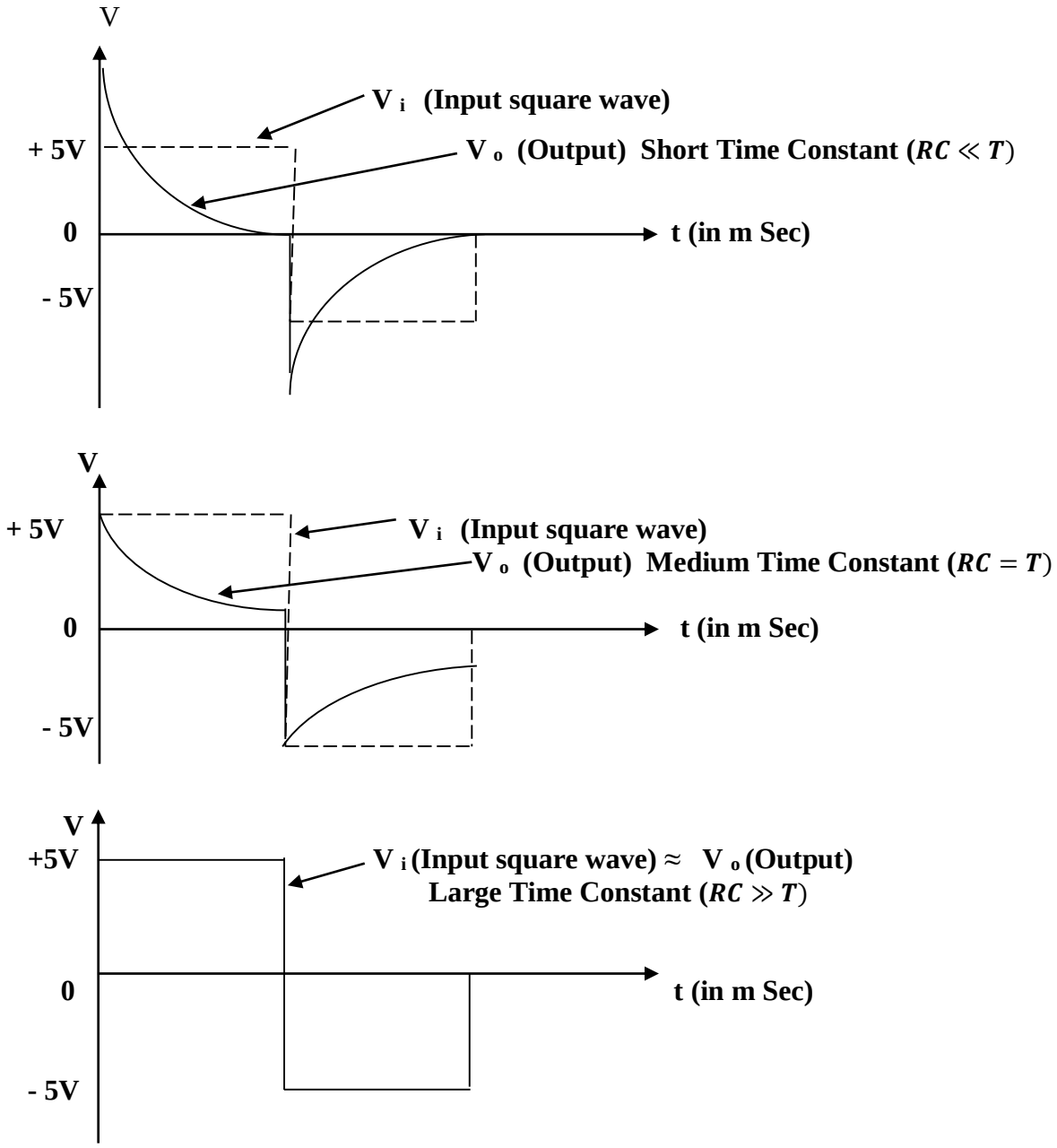
i) RC INTEGRATOR (or) LOW PASS FILTER:







ii) **RC DIFFERENTIATOR (or) HIGH PASS FILTER:**



RESULT:

Hence the RC Integrator & RC Differentiator circuits were designed and output waveforms are verified.

Exp No: 2 **Date:**

NON LINEAR WAVE SHAPING – CLIPPERS

AIM:

To design and verify waveforms of different clipping circuits with different reference voltage.

COMPONENTS REQUIRED:

1. Resistors 1kΩ (1No.)
2. Diode 1N4007 (2No.)
3. Bread Board
4. Connecting wires
5. CRO & Probes
6. Function Generator
7. Regulated Power Supply (0 - 30V)

THEORY: The non-linear semiconductor diode in combination with resistor can function as clipper circuit. Energy storage components like capacitor etc. are not required in the basic process of clipping. These circuits will select part of an arbitrary waveform which lies above or below some particular reference voltage level and that selected part of the waveform is used for transmission. So they are referred as voltage limiters, current limiters, amplitude selectors or slicers.

There are three different types of clipping circuits.

1) Positive Clipping circuit.

2) Negative Clipping.

3) Positive and Negative Clipping (slicer).

In positive clipping circuit positive cycle of Sinusoidal signal is clipped and negative Portion of sinusoidal signal is obtained in the output. If reference voltage is added, instead of complete positive cycle that portion of the positive cycle which is above the reference voltage value is clipped.

In negative clipping circuit instead of positive portion of sinusoidal signal, negative Portion is clipped.

In slicer both positive and negative portions of the sinusoidal signal are clipped.

Operation can be explained based on equations as shown below:

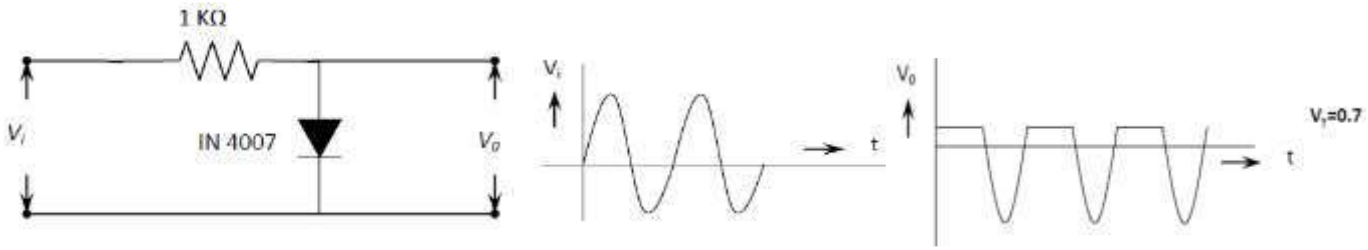
1. When $V_i < V_R + V_\gamma$, Diode is reverse biased (OFF). Output follows the input.
2. When $V_i > V_R + V_\gamma$, Diode is forward biased (ON). And the Output is equal to $(V_R + V_\gamma)$.

Here V_i is Supplied input voltage, V_R is connected reference voltage, V_γ is diode cut-in voltage

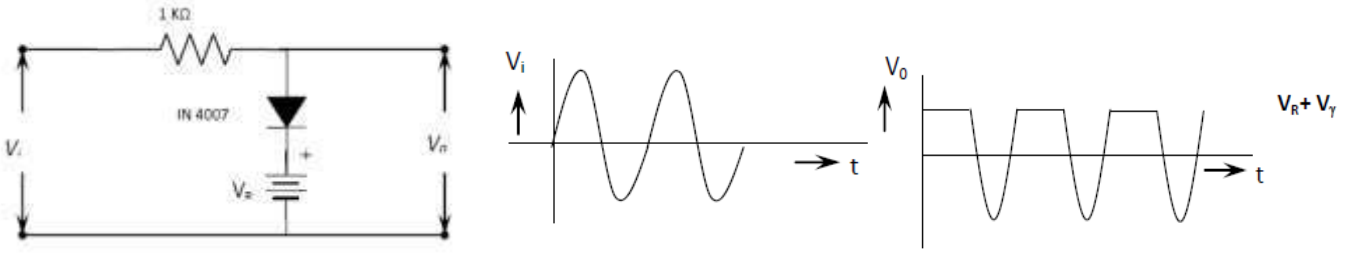
CIRCUIT DIAGRAMS **MODEL GRAPHS**

Input Waveforms **Output waveforms**

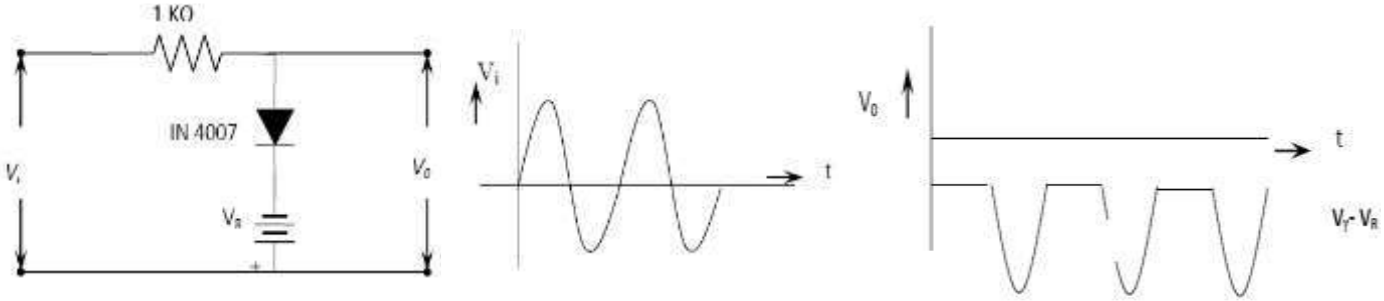
1) Positive clipper:



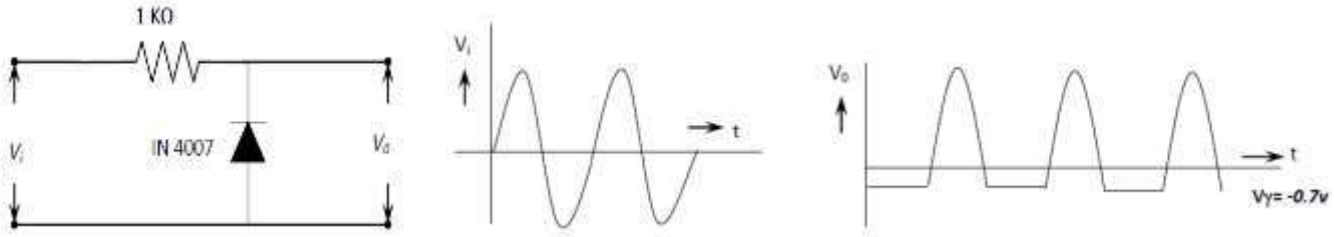
2) Positive clipper with positive reference voltage:



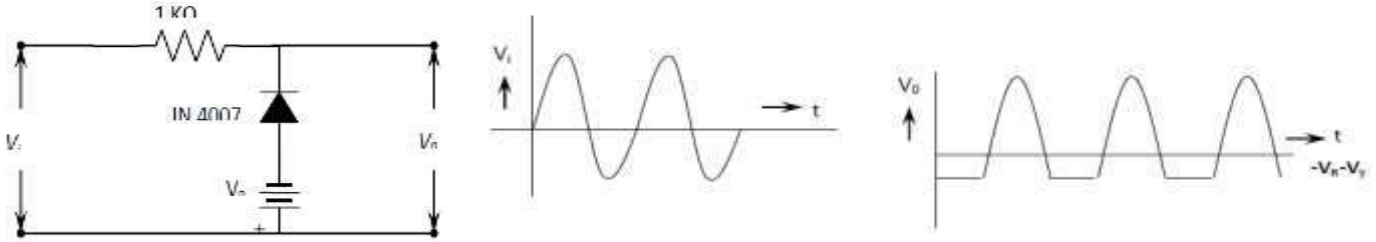
3) Positive clipper with negative reference voltage:



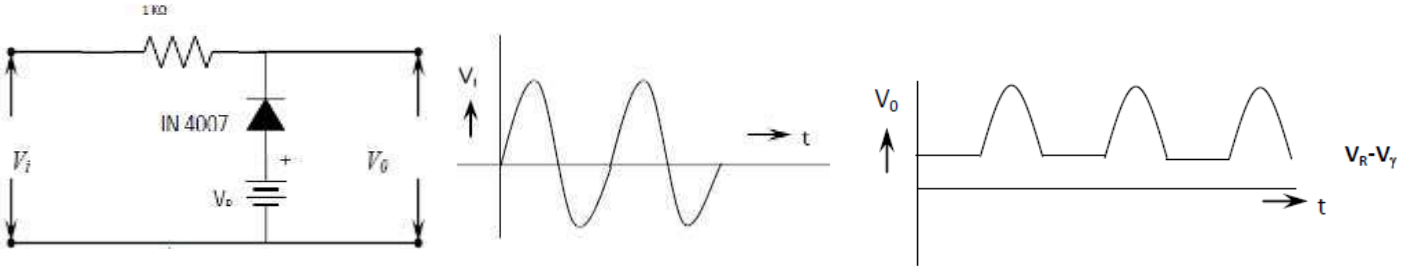
4) Negative clipper:



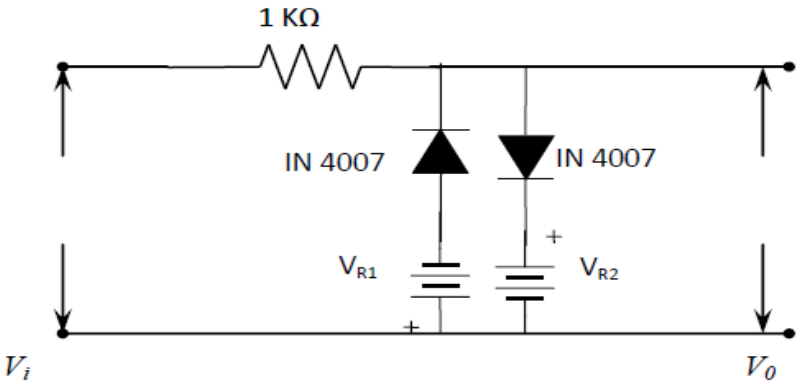
5) Negative clipper with negative reference voltage:

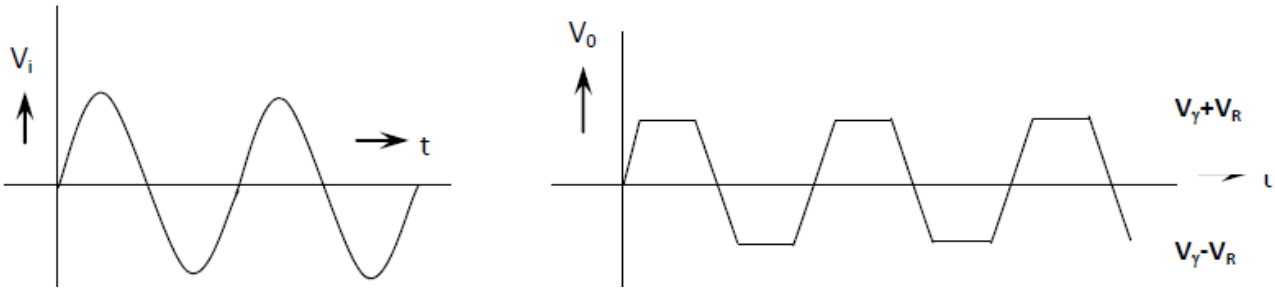


6) Negative clipper with positive reference:



7) Slicer (Two level clippers):





Tabular column:

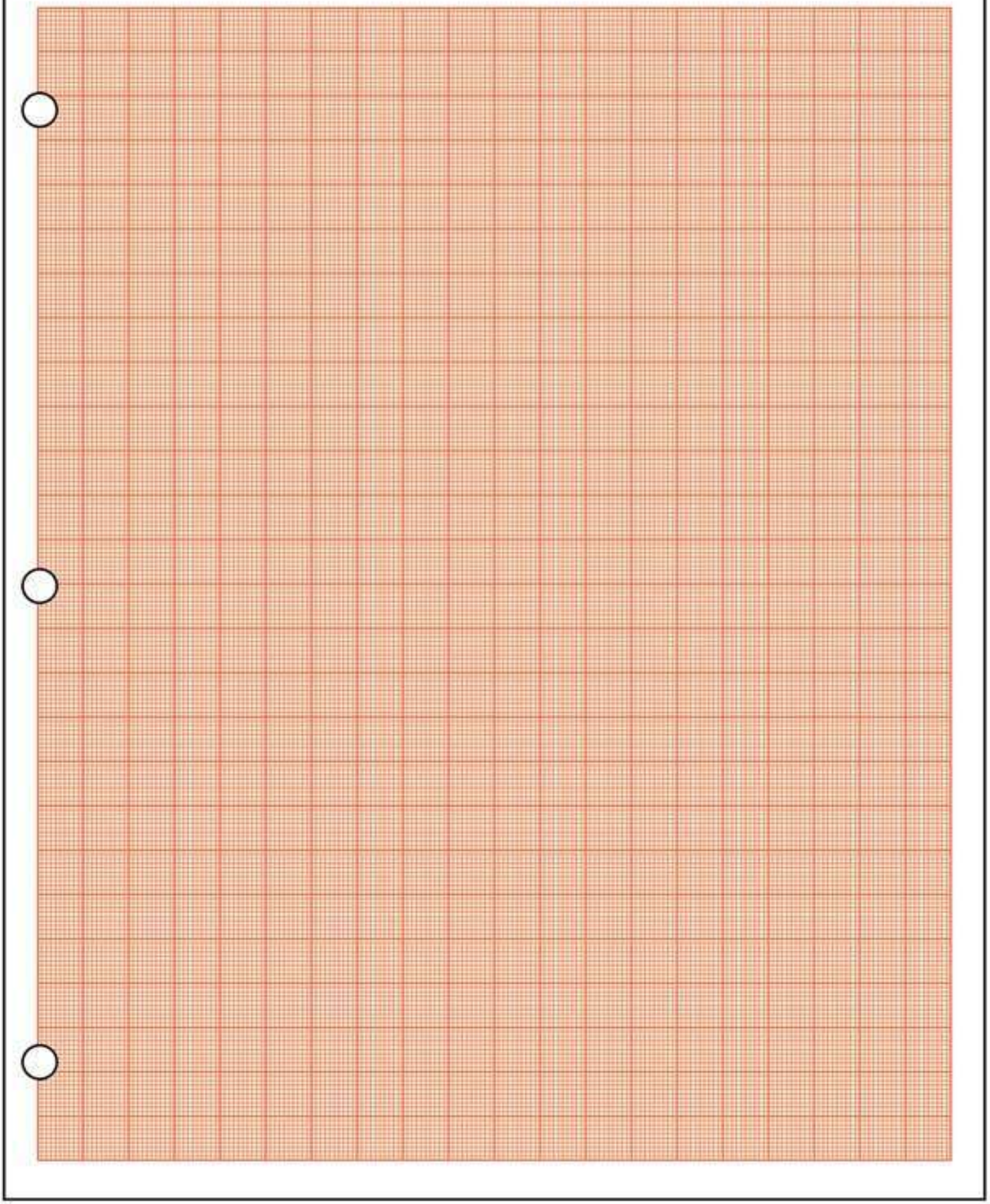
	THEORETICAL VALUE	PRACTIAL VALUE
I. Positive Clipping	V_γ=0.7V	
II. Positive Clipping with Positive Reference Voltage	$V_R + V_\gamma$ =0.7+2V=2.7V	
III. Positive Clipping with Negative Reference Voltage	V_γ-V =-0.7v+2v =1.3v	
IV. Negative Clipping	Vγ= -0.7v	
V. Negative Clipping with Positive Reference Voltage	$-V_R-V_\gamma$ -0.7v-2v -2.7v	
VI. Negative Clipping with Negative Reference Voltage	V_R-V_γ 2v-0.7v 1.3v	
VII. Slicer	$V_\gamma+V_R$ =0.7v+2v =2.7v $V_\gamma-V_R$ =0.7v-2v =-1.3v	

PROCEDURE:

1. Connect the circuit elements as shown in the Circuit Diagram.
2. A Sinusoidal voltage of 10V and frequency of 1kHz is applied to the circuit as an input.
3. Note down the corresponding output wave forms from C.R.O and Enter the values in table.
4. Plot the graph from above readings.

RESULT:

Hence different clipping circuits were designed and corresponding outputs were verified.



Exp No: 3 **Date:**

NON LINEAR WAVE SHAPING – CLAMPERS

AIM:

To design and verify the characteristics of different clamping circuits with different reference voltage.

COMPONENTS REQUIRED:

1. Capacitor 10 μ F (1 No)
2. Diode IN4007 (1 No)
3. Bread Board
4. Connecting wires
5. CRO & Probes
6. Function Generator

THEORY:

"A clamping circuit is one that takes an input waveform and provides an output that is a faithful replica of its shape but has one edge tightly clamped to the zero voltage reference point".

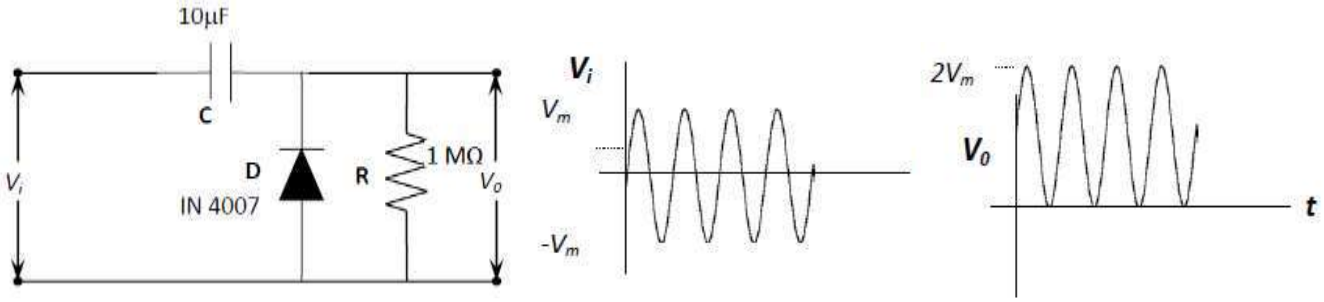
There are various types of Clamping circuits, which are mentioned below:

1. Positive Clamping Circuit.
2. Negative Clamping Circuit.
3. Positive Clamping with positive reference voltage.
4. Negative Clamping with positive reference voltage.
5. Positive Clamping with negative reference voltage.
6. Negative Clamping with negative reference voltage.

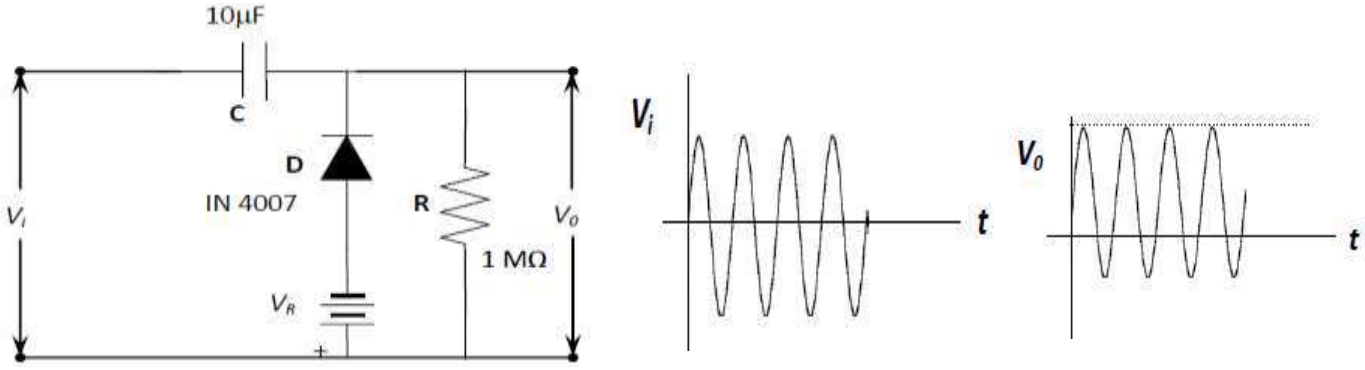
CIRCUIT DIAGRAM: **MODEL GRAPH:**

INPUT WAVEFORM **OUTPUT WAVEFORM**

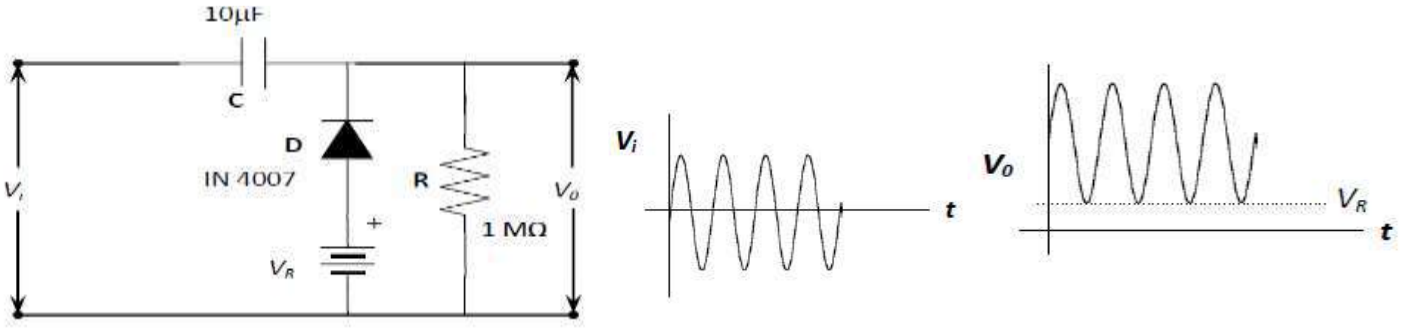
1. Positive Clamping Circuit:



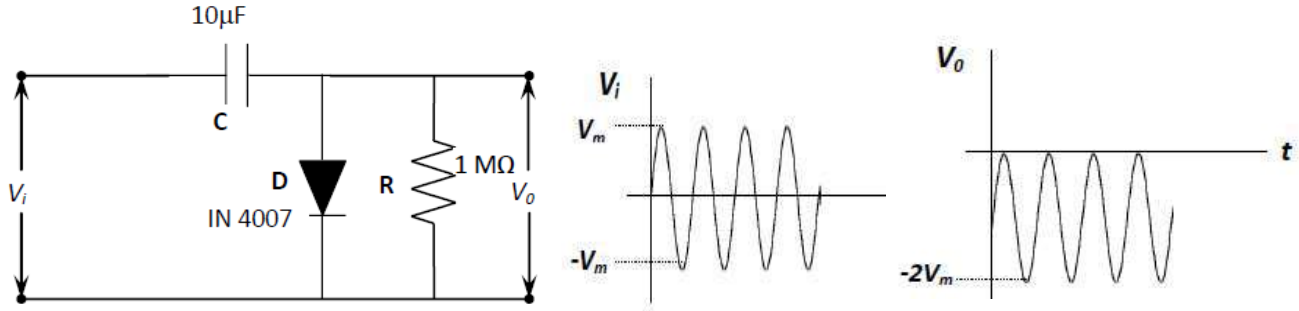
2. Positive Clamping with negetive reference voltage:



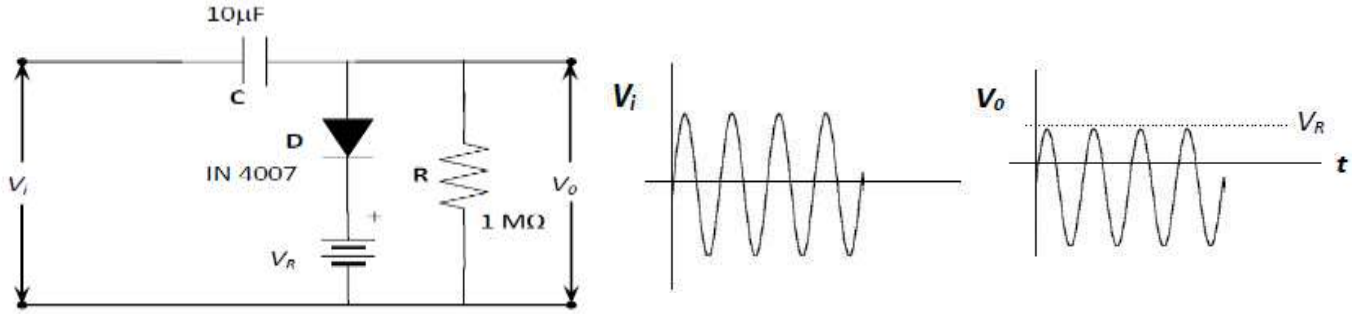
3. Positive Clamping with Positive reference voltage:



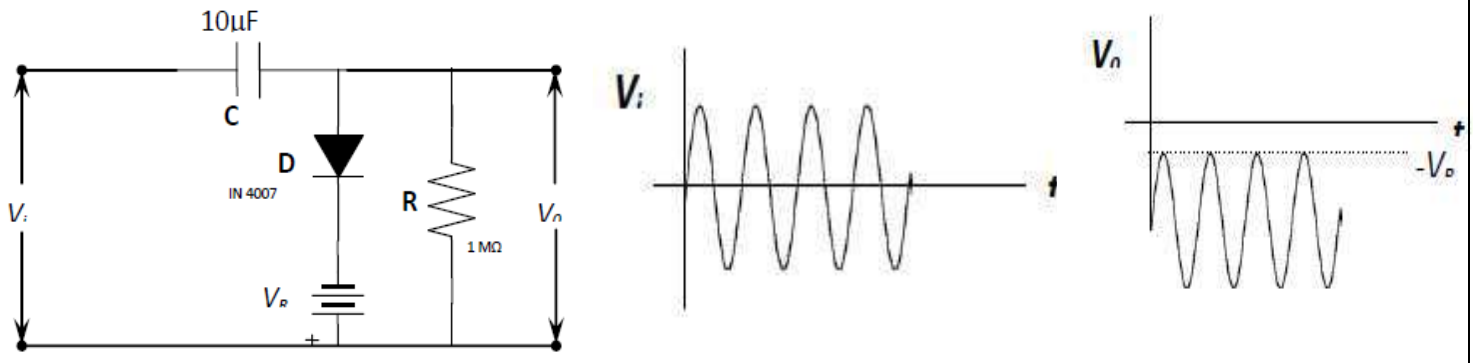
4. Negative Clamping Circuit:



5. Negative Clamping with positive reference voltage:



6. Negative Clamping with negative reference voltage:

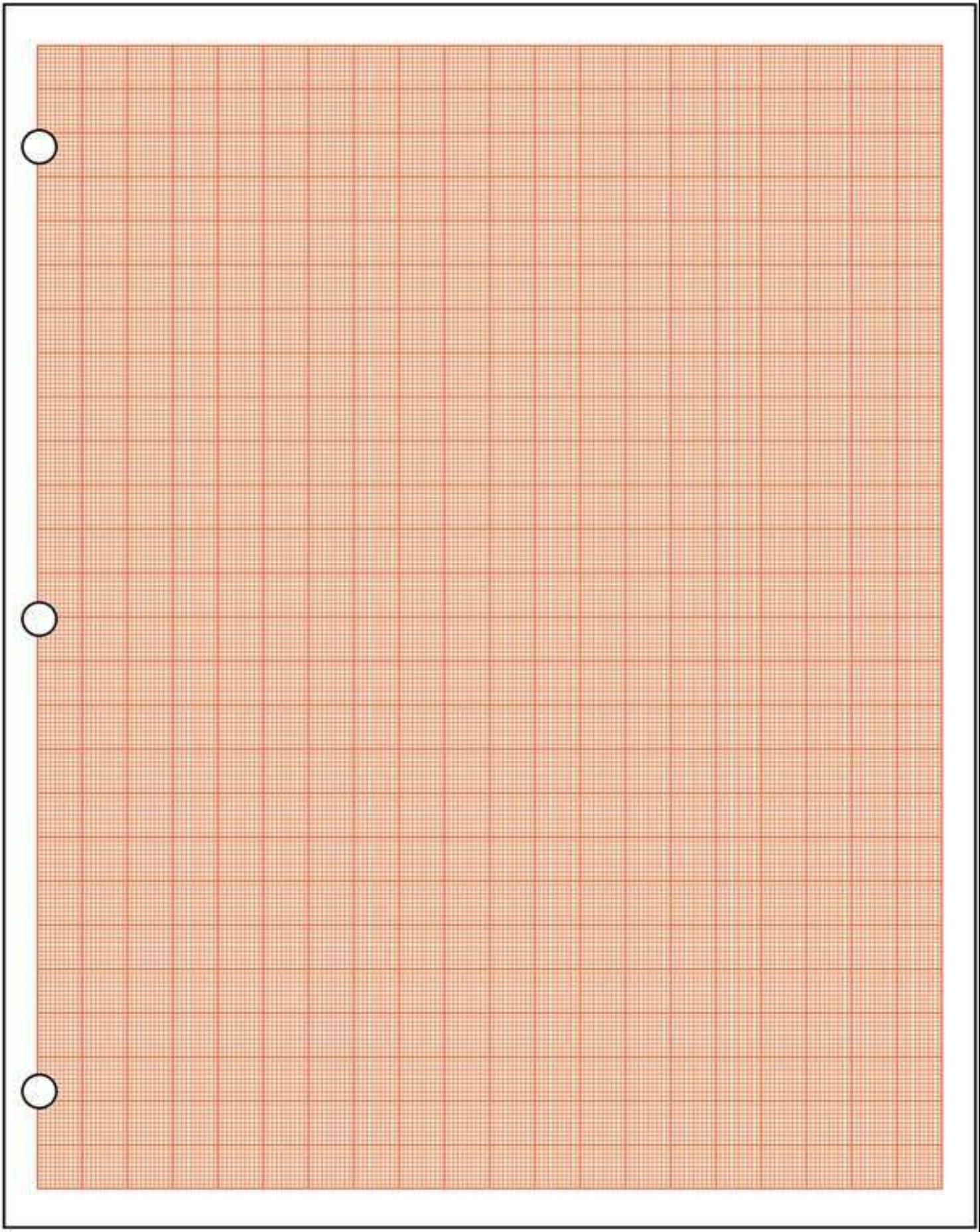


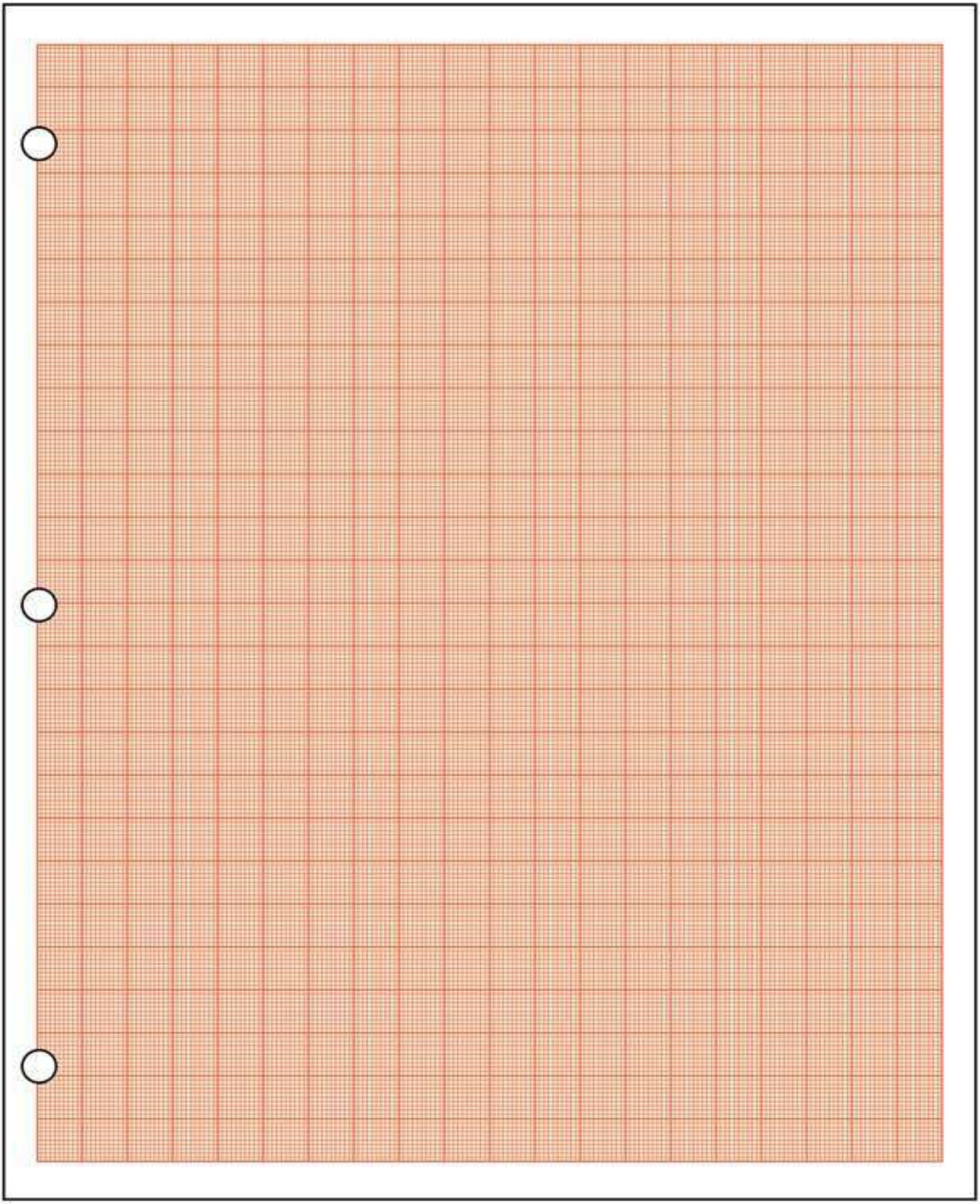
PROCEDURE:

1. Connect the circuit elements as shown in the Circuit Diagram.
2. A Sinusoidal voltage of 10V and frequency of 1kHz Hz is applied to the circuit as an input.
3. Note down the corresponding output wave forms in C.R.O and plot the graph.

RESULT:

Hence different clamping circuits were designed and outputs were verified.





Exp No: 4 **Date:**

TRANSISTOR AS A SWITCH

AIM:

To construct and verify the switching characteristics of the transistor.

COMPONENTS REQUIRED:

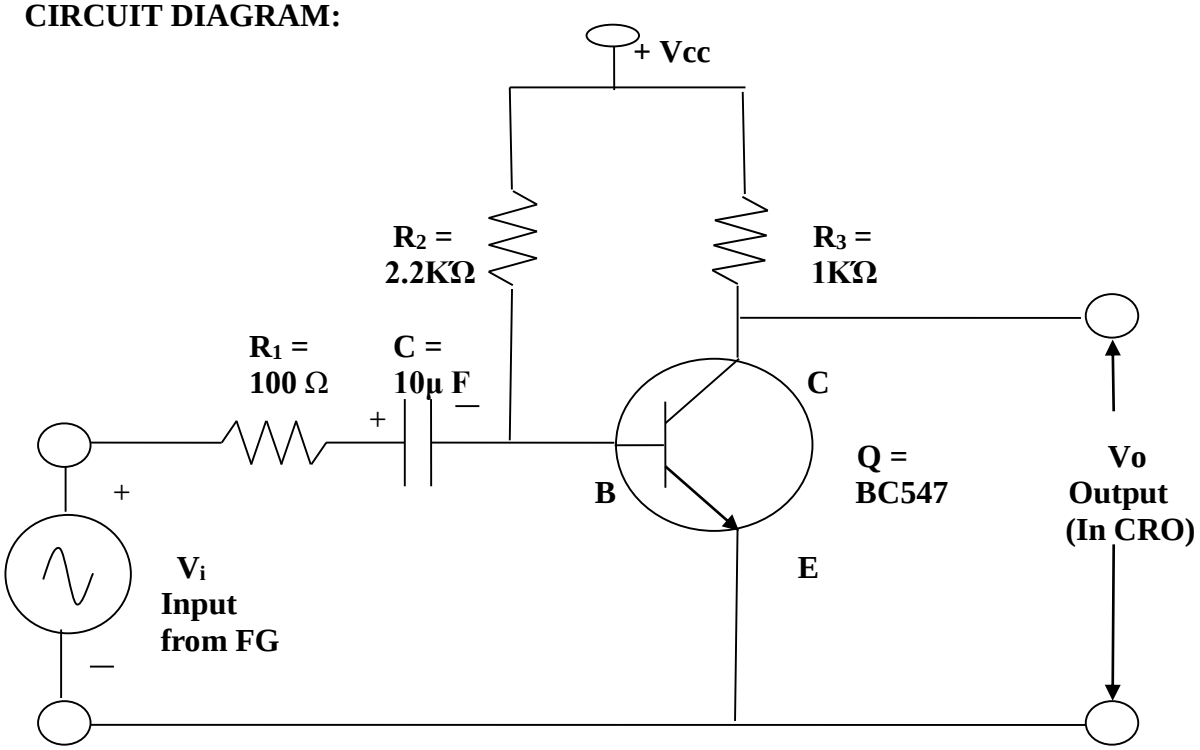
1. Transistor BC 547 ---------- 1No
2. Capacitor 10 μ F ----------1No
3. Resistors 100Ω, 1K Ω, 2.2KK Ω ---- 1No each
4. Bread Board
5. Connecting wires as required
6. CRO & Probes
7. Function Generator
8. Regulated Power Supply (0 - 30V)

THEORY:

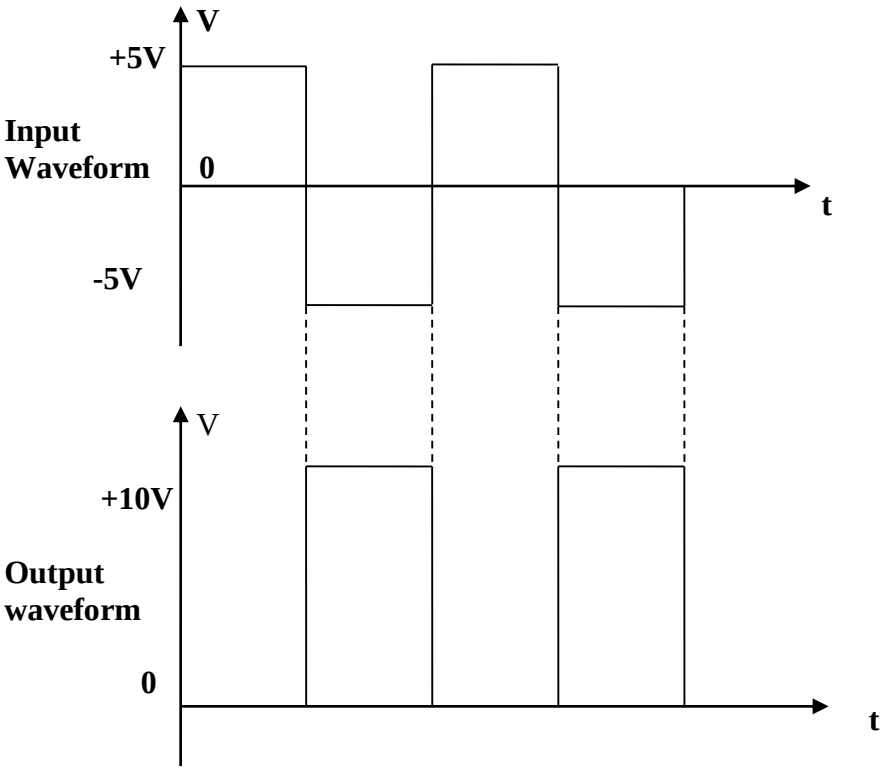
The operation of a transistor as a switch can be illustrated using circuit diagram. When the input voltage is negative or zero, then is in cut off and so no current flows through RC. Hence the output voltage is equal to V_{cc}. When its voltage jumps to the voltage "V", the transistor will be drawn into saturation.

Thus the transistor can turn off depending upon whether input voltage is positive or negative. Thus the transistor can acts as a switch. When no signal is applied the transistor will be held in saturation by the connection of base to supply voltage through the resistor.

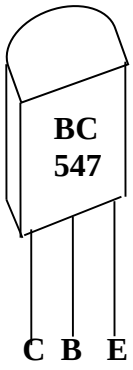
CIRCUIT DIAGRAM:



MODEL GRAPH:



TRANSISTOR PIN DETAILS:



PROCEDURE:

1. Connect the circuit elements as shown in the Circuit Diagram.
2. Applying the square wave voltage of 10V and frequency of 1kHz Hz is applied to the circuit as an input.
3. Observe the corresponding output wave form at the collector of the transistor.
4. Note down the corresponding values from C.R.O and plot the graph.

RESULT:

The switching characteristics of the transistor are verified and output waveform is plotted.

Exp No: 5 **Date:**

STUDY OF LOGIC GATES

AIM:

To verify the truth tables of different logic gates.

COMPONENTS REQUIRED:

1. IC's 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86 (each 1No)
2. Light Emitting Diode (LED)
3. Bread Board
4. Connecting wires as required
5. Fixed Power Supply (0 - 5V)

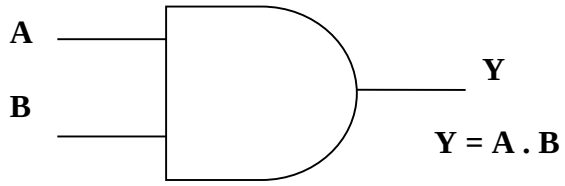
THEORY:

A logic gate is an electronic circuit which makes logical decisions. To arrive at this decisions, the most common logic gates used are OR, AND, NOT, NAND, and NOR gates. The NAND and NOR gates are called as the universal gates. The exclusive OR gate is another logic gate which can be constructed during basic gates such as AND, OR and NOT gates.

Logic gates have two or more inputs and only one output except for the NOT gate, which has only one input. The output signal appears only for certain combinations of the input signal. The manipulation of binary information is done by the gates. The logic gates are the building blocks of hardware which are available in the form of various IC families. Each gate has a distinct logic symbol and its operation can be described by means of an algebraic function. The relationship between the input and output variables of each gate can be represented in tabular form called truth table.

AND: This operation is represented as 'dot'. The IC number of AND gate is 74LS08. The output of logical operation AND is 1 if and only if both inputs are 1 in all other cases it is 0.

$$Z = A \cdot B$$

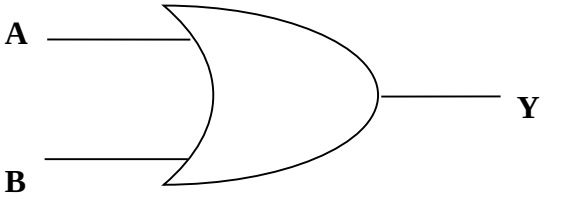


74 LS 08

Inputs		Output
A	**B**	**Y**
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

OR: This operation is represented as 'plus'. The IC number of OR gate is 74LS32. The output of logical operation OR is 1 if any one of the input is 1. If both the inputs are 0, the output is 0.

$$Z = A + B$$



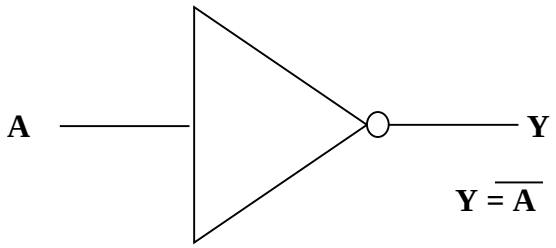
Y = A + B

74 LS 32

Inputs		Output
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**1**

NOT: This operation is represented by a 'bubble' before a common gate. The IC number of NOT gate is 74LS04. The output NOT gate is 1 if the input is 0 and vice versa

$$Z = \overline{A}$$



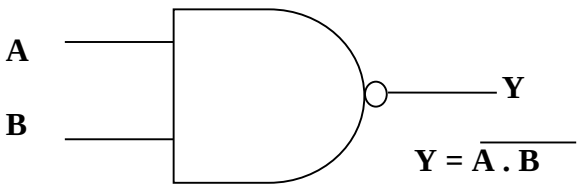
$Y = \overline{A}$

74 LS 04

Input	Output
A	**Y**
0	**1**
1	**0**

NAND: This operation is a compliment of the AND function. It is graphically represented by an AND gate followed by a bubble. The IC number of NAND gate is 74LS00. The output is 1, if any of the input is 1.The output is 0 if both the inputs are 0.

$$Z = \overline{A \cdot B}$$



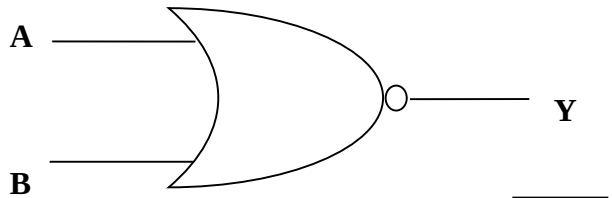
$Y = \overline{A \cdot B}$

74 LS 00

Inputs		Output
A	**B**	**Y**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

NOR: This operation is a compliment of the OR function. It is graphically represented by an OR gate followed by a bubble. The IC number of NOR gate is 74LS02. The output of logical operation NOR is 0, if any one of the input is 1. The output is 1, if both the inputs are 0.

$$Z = \overline{A + B}$$



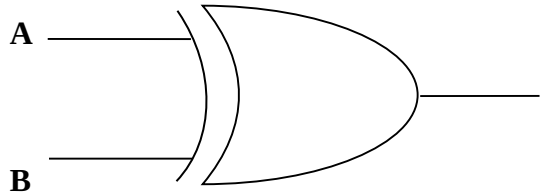
Y = $\overline{A + B}$

74 LS 02

Inputs		Output
A	**B**	**Y**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

EX - OR: The EXCLUSIVE – OR gate has a graphic symbol similar to that of OR gate except for the additional curved lines on the input side. If both the inputs are same the output is 1 otherwise the output is 0.

$$Z = \overline{A} \cdot B + \overline{B} \cdot A$$



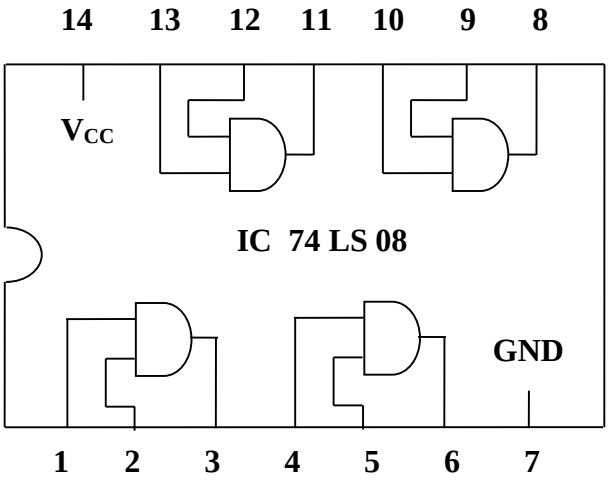
Y = A $\oplus$ B

74 LS 86

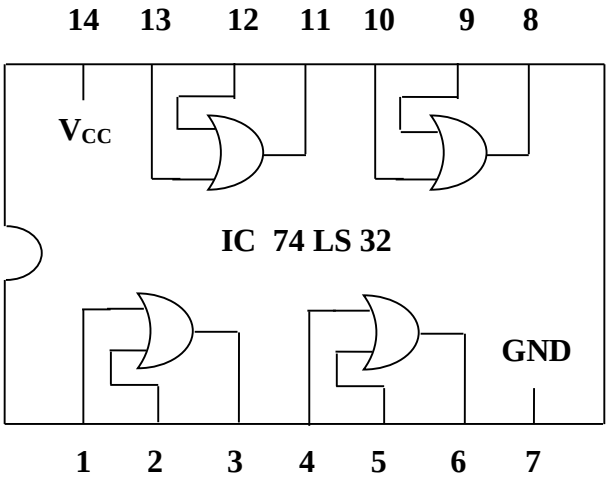
Inputs		Output
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

PIN DIAGRAMS OF ALL LOGIC GATES:

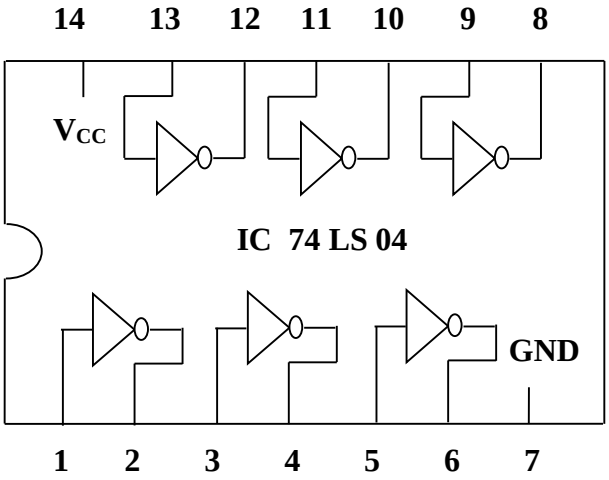
AND GATE



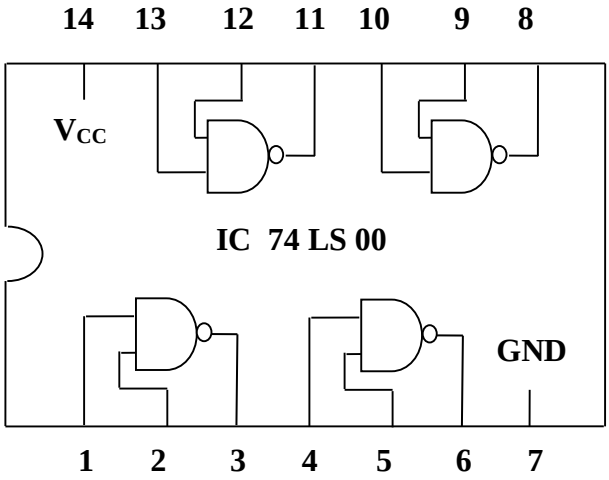
OR GATE



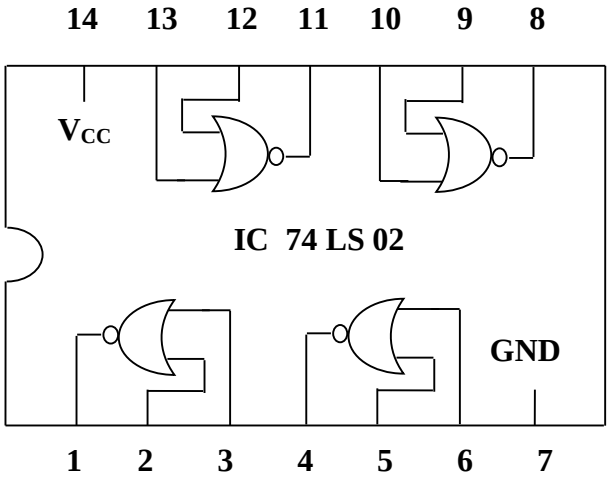
NOT GATE



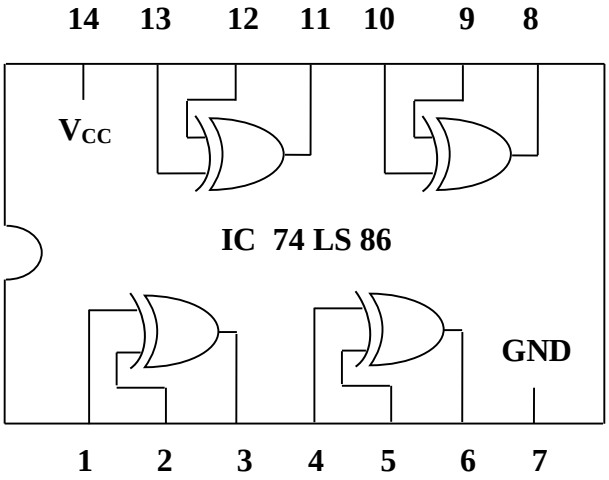
NAND GATE



NOR GATE



EX - OR GATE



PROCEDURE:

1.The IC's are placed on the bread board.

2. A voltage of +5V is applied to pin no.14 and –Ve is applied to pin no.7.

3. Inputs and Outputs are connected according the gates which are taken.

4. For the input 1 we have to connect the input terminal to +5V and for 0 to –Ve.

5. Output is verified in LED. If the LED is ON the output is 1, if OFF output is 0.

6. According to the Logic gates truth table we have to verify the inputs and outputs.

RESULT:

The truth tables of different Logic gates are verified.

Exp No: 6 **Date:**

HALF ADDER AND FULL ADDER

AIM:

To design and verify the truth tables of Half adder & Full adder circuits.

COMPONENTS REQUIRED:

1. Light Emitting Diode (LED)
2. Bread Board
3. Connecting wires as required
4. Fixed Power Supply (0 - 5V)
5. IC's 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86 (each 1No)

THEORY :

Half Adder:

A logic circuit used for the addition of two one-bit numbers is referred to as half adder.

It consist of an EX-OR gate(Output is sum) and AND gate(Output is carry).

CARRY $C = A \cdot B$

SUM $S = A\,\overline{B} + \overline{A}\,B = A \oplus B$

Full adder:

A logic circuit which is used for the addition of three bits is full adder

Let A, B, C are the three inputs of full adder. Outputs are Sum and Carry which are given by

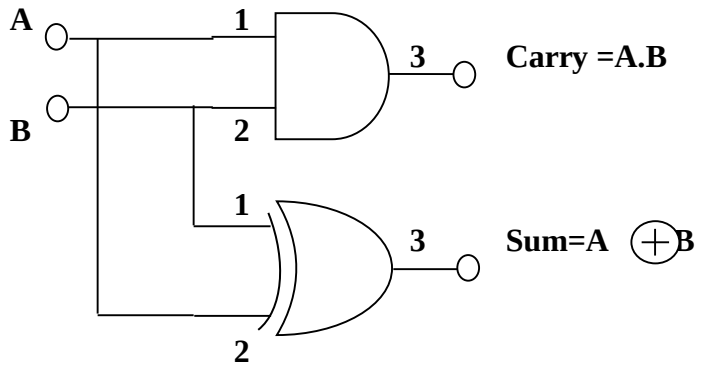
$Sum = A \oplus B \oplus C$

$Carry = A \cdot B + C\,(A \oplus B)$

CIRCUIT DIAGRAM:

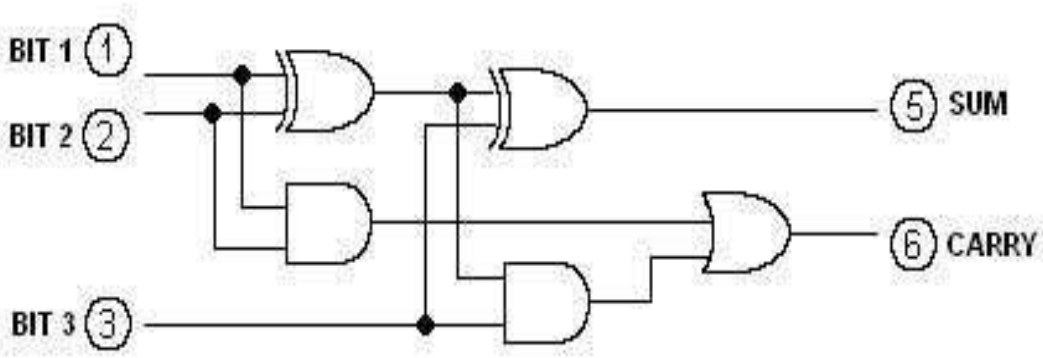
TRUTH TABLES

Half Adder:



Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder: A = Bit 1, B = Bit 2, C= Bit 3



BITS				
1	2	3	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Sum = A ⊕ B ⊕ C

Carry = A . B + C (A⊕B)

RESULT:

The truth tables of half adder and full adder are verified.

Exp No: 7 **Date:**

SAMPLING GATES

AIM:

To construct and verify the Sampling Gates and its output waveform.

COMPONENTS REQUIRED:

1. Diode 1N4007 ---------- 1 No
2. Capacitor 0.01 μF ---------- 1 No
3. Resistors 1 KΩ ---------- 2 No's
4. Bread Board
5. Connecting wires as required
6. CRO & Probes
7. Function Generators

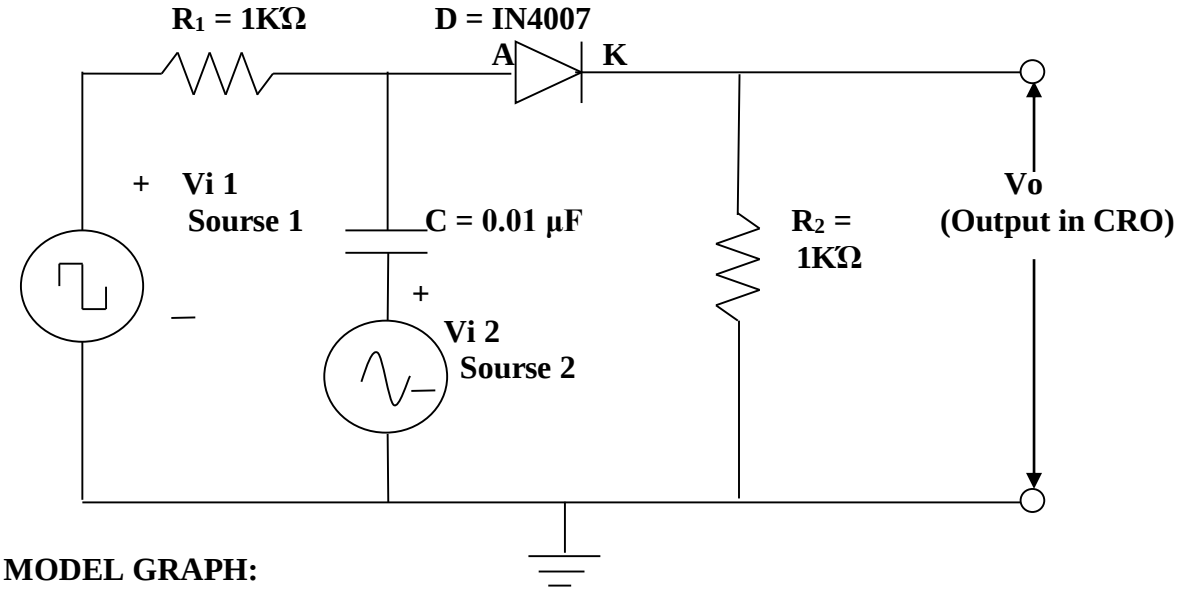
THEORY:

A Sampling gate is basically a transmission circuit, which allows an input signal to pass through it during a selected interval and block its passage outside this time interval. A sampling gate is sometimes referred to as time-selection gates.

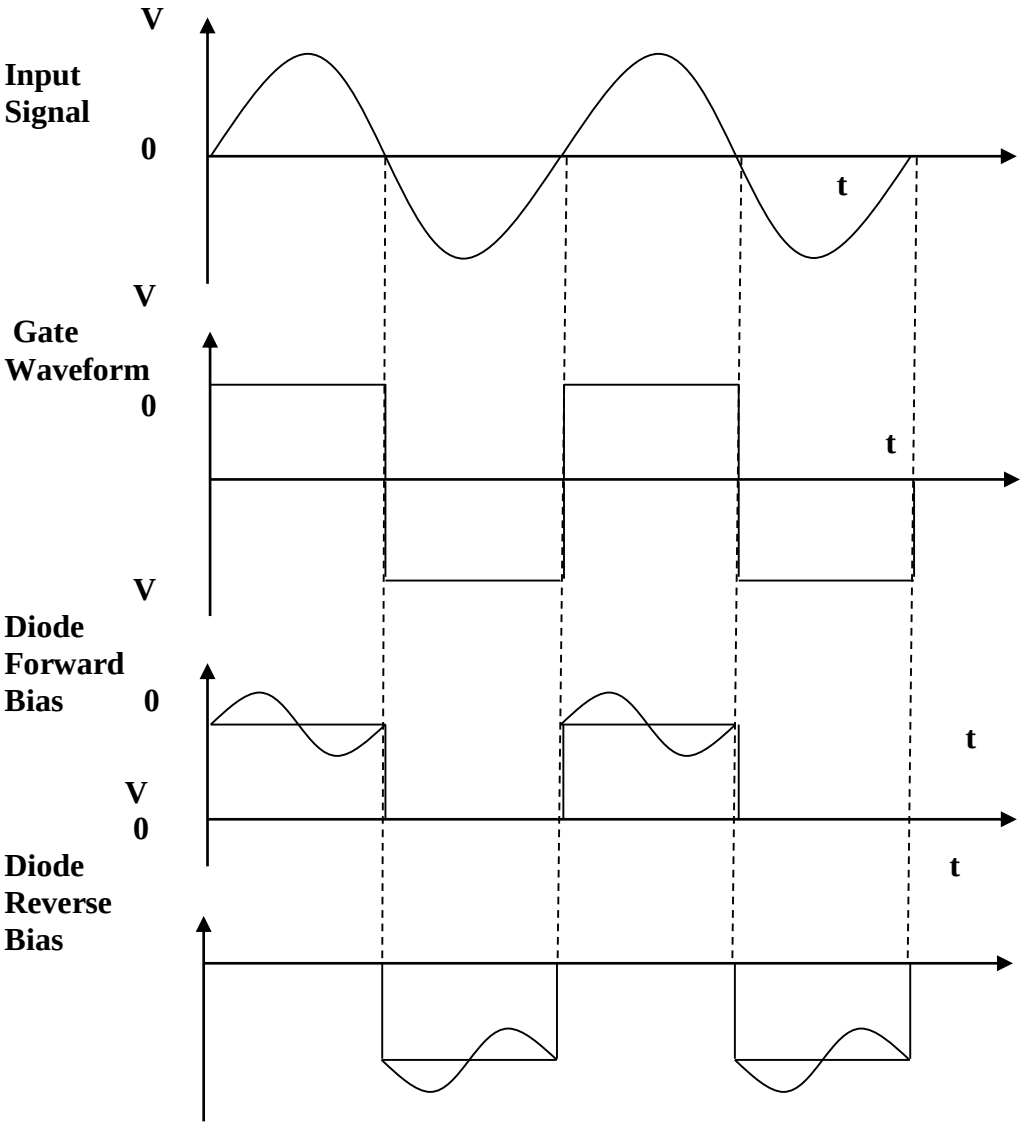
The circuit uses a diode D, with certain polarity, a capacitor C and resistors R_1 and R_L. Capacitor C_1 and R_1 from together an integrating circuit, with the voltage levels V_1 and V_2 the diode gets heavily reverse biased respectively.

With the diode reverse biased, there is no conduction and hence the output is zero. This is equivalent to the open switch. When the gate voltage rises abruptly from V_1 to V_2 , the positive going input signal causes the diode to be forward biased. The diode conducts and the input voltage across R_L. If the conditions are assumed to be ideal, then there is neither attenuation nor distortion of the input signal. The output voltage would be an exact replica of the input signal.

CIRCUIT DIAGRAM:



MODEL GRAPH:

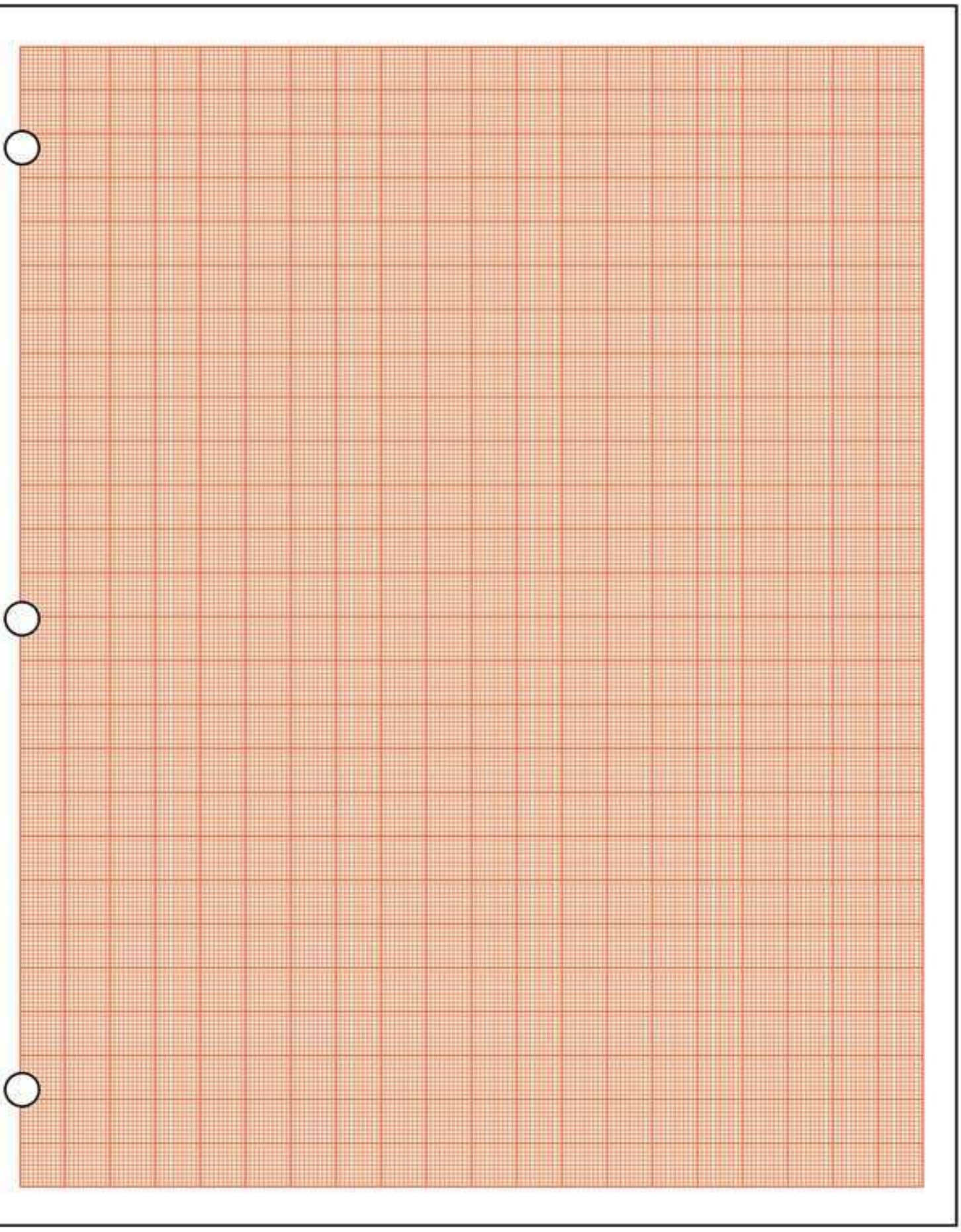


PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. The square wave signal of 4 volts is to be applied at the resistor R_1.
3. The another signal of sine wave signal of 4 volts is to be applied at the capacitor C.
3. Obtain the output wave forms for the given input signals across the resistor R_2 from the CRO and the graph was plotted.

RESULT:

The Sampling Gates was constructed and the output wave forms are verified.



Exp No: 8 **Date:**

ASTABLE MULTIVIBRATOR

AIM:

To study and verify the characteristics of an astable multivibrator.

COMPONENTS REQUIRED:

1. Transistor BC 547 ---------- 2 No's
2. Capacitor 0.01 μ F ----------2 No's
3. Resistors 1K Ω, 33K Ω ------- each 1No
4. Bread Board
5. Connecting wires as required
6. CRO & Probes
7. Function Generator
8. Regulated Power Supply (0 - 30V)

THEORY:

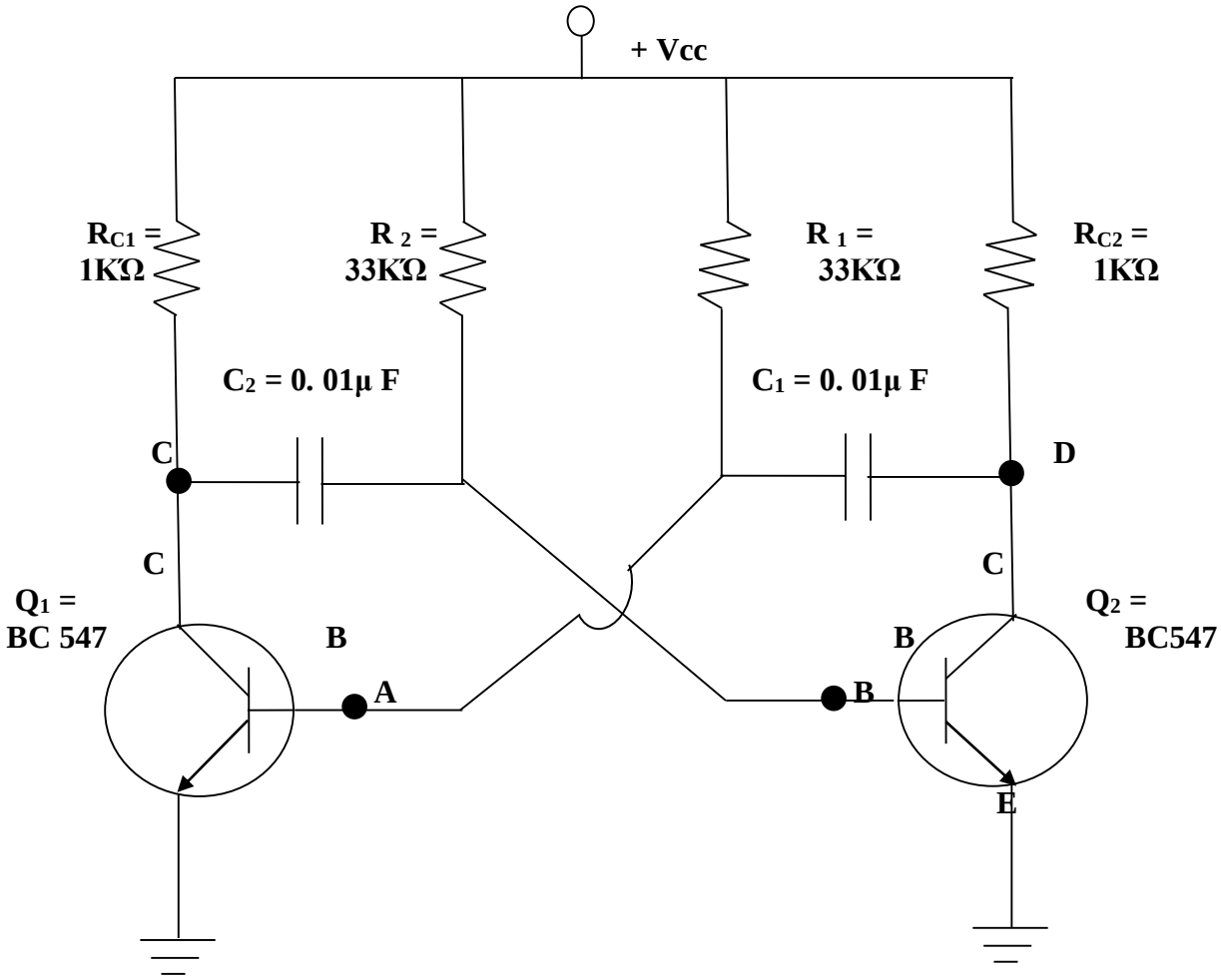
Astable multivibrator has two quasi – states and it keeps on vibrating between these two states by itself. No external signal is needed. The astable remains indefinitely in any of these two states.

Assuming that the multivibrator is already in action and is switching between two states. Let it be further observed that at the instant considered Q_1 is OFF and Q_2 is ON. Since Q_2 is ON, the capacitor is charged through RC_1 and capacitor C_1 discharges through R_1 the voltage across C_1 when it is about to start discharging in V_{cc}.

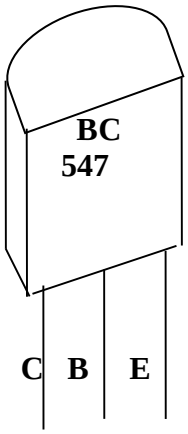
As capacitor C_1 discharges more and more the identical at the point A becomes more and more positive, and eventually $V_A = V_r$ the cut in voltage Q_1 states conducting. When Q_1 is ON Q_2 becomes OFF.

Similar operation repeats when Q_1 becomes ON and Q_2 becomes OFF and vice versa.

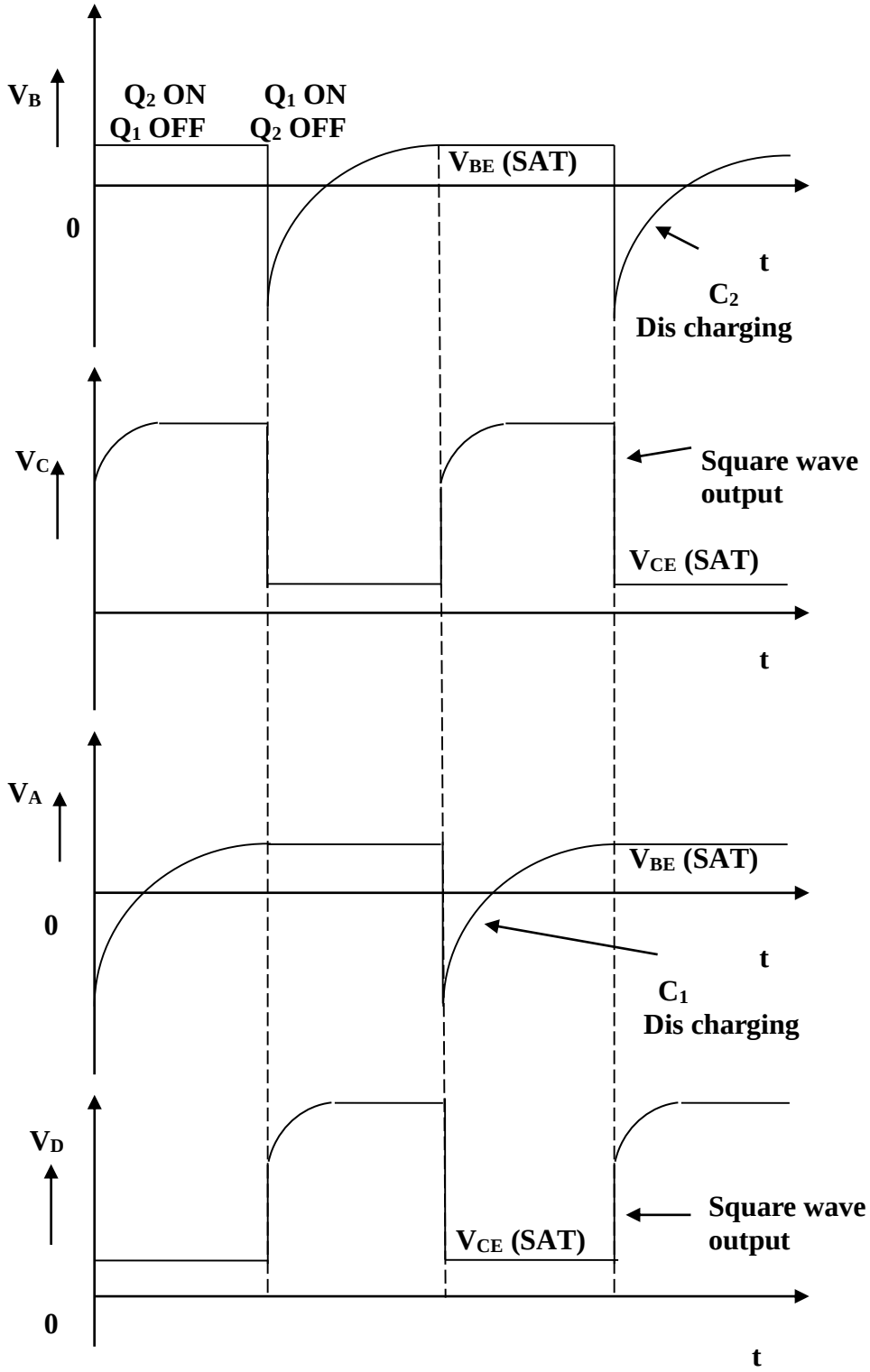
CIRCUIT DIAGRAM:



TRANSISTOR PIN DETAILS:



MODEL GRAPH:


V_B
Q_2 ON
Q_1 OFF
Q_1 ON
Q_2 OFF
V_{BE} (SAT)
0
t
C_2
Dis charging
V_C
Square wave
output
V_{CE} (SAT)
t
V_A
V_{BE} (SAT)
0
t
C_1
Dis charging
V_D
Square wave
output
V_{CE} (SAT)
0
t

V_B = Input Voltage at base of Q_2

V_C = Input Voltage at collector of Q_1

V_A = Input Voltage at base of Q_1

V_D = Input Voltage at collector of Q_2

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Take the output across the collector considering Q1 is OFF and Q_2 is ON, we get V_{c2}.
3. Now connect the wire across the base also and take the output V_{B2} and repeat with Q_1 ON and Q_2 OFF.
4. The required waveforms are taken from the CRO.

RESULT:

The astable multivibrator is studied and its output waveforms were verified.

Exp No: 9 **Date:**

MONOSTABLE MULTIVIBRATOR

AIM:

To conduct and verify the monostable multivibrator and draw the waveforms.

COMPONENTS REQUIRED:

1. Transistor BC 547 ---------- 2 No's
2. Capacitor 0.1 μF ---------- 2 No's
3. Resistors 1 KΩ ---------- 2 No's
   10 KΩ ---------- 4 No's
4. Diode 1N 4007 ---------- 1 No
5. Bread Board
6. Connecting wires as required
7. CRO & Probes
8. Function Generator
9. Regulated Power Supply (0 - 30V)

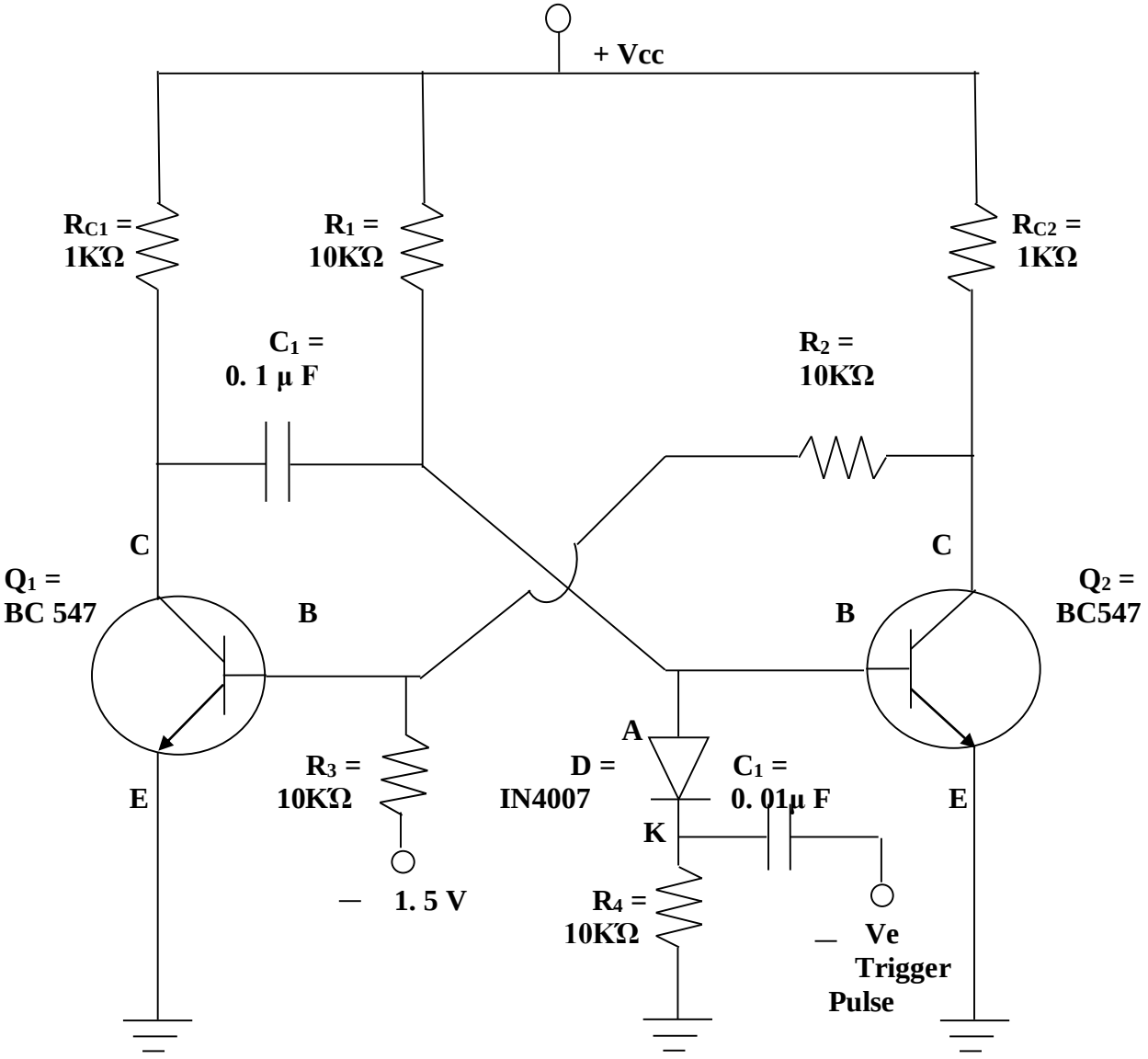
THEORY:

A monostable multivibrator has one stable state and the other state being quasi – stable state. Normally the multi is in the stable state and when an external triggering pulse is applied it switches back to its original state, without any triggering pulse.

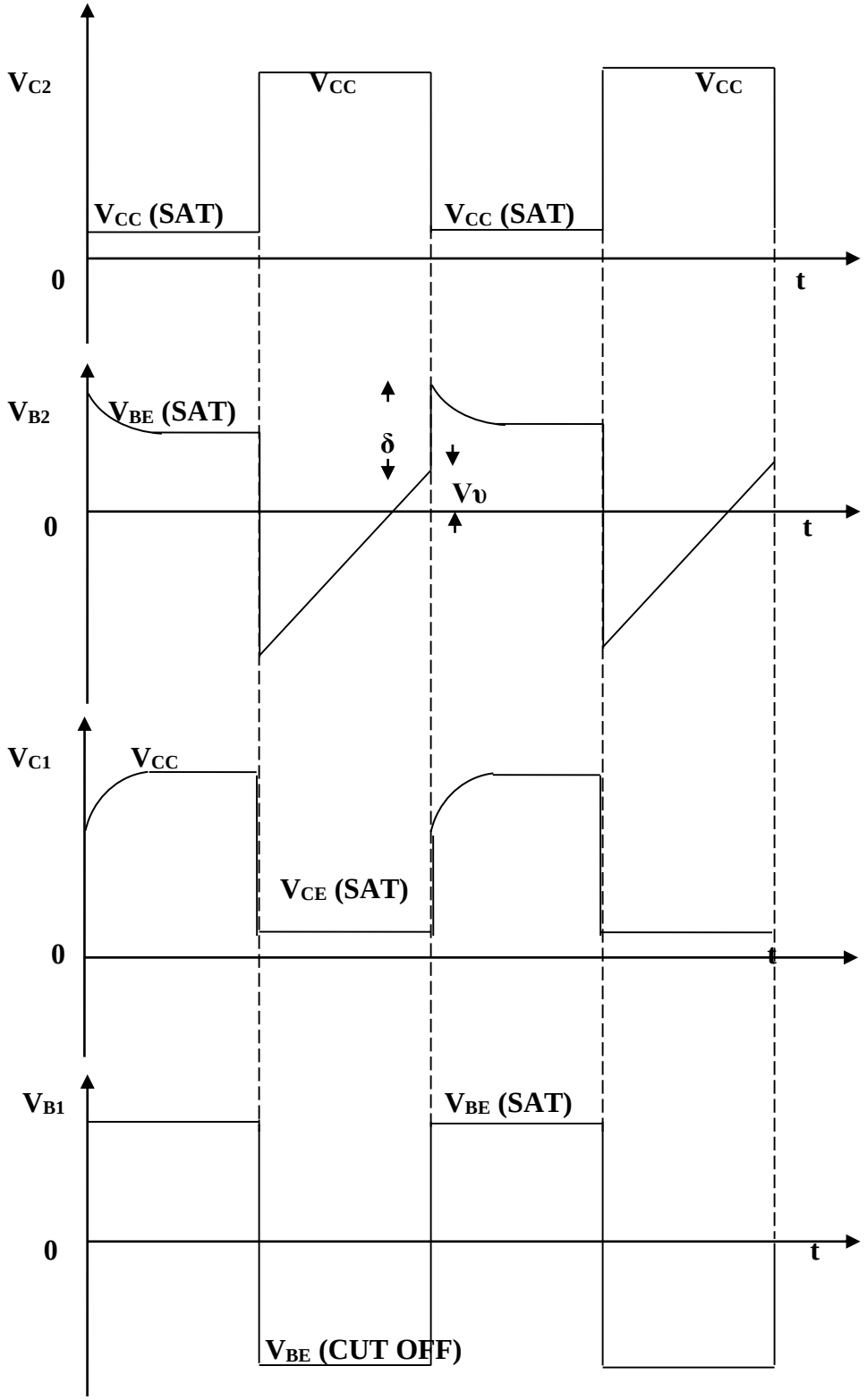
The output of the monostable multi while it remains in the quasi – stable is a part of duration T, whose value depends upon the circuit components. Hence the monostable multivibrator is called as 'pulse operator '.

The monostable multivibrator is also referred to and 'one shot' or 'uni vibrator'. Since only one triggering signal is required to revert to the original state of stability, that is the stable state.

CIRCUIT DIAGRAM:



MODEL GRAPH:


V_{C2}
V_{CC}
V_{CC}
V_{CC} (SAT)
V_{CC} (SAT)
0
t
V_{B2}
V_{BE} (SAT)
δ
Vυ
0
t
V_{C1}
V_{CC}
V_{CE} (SAT)
0
t
V_{B1}
V_{BE} (SAT)
0
t
V_{BE} (CUT OFF)

V_{C2} = Voltage at collector of Q_2
V_{B2} = Voltage at base of Q_2
V_{C1} = Voltage at collector of Q_1
V_{B1} = Voltage at base of Q_1

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Usually a +Ve supply voltage of about 10 V is applied as source voltage to V_{cc}
3. In the normal operation transistor Q_2 is ON and output voltage across the base and collector are noted.
4. Then an external triggering is applied from the high-pass filter circuit.
5. Then the transistor Q_2 is OFF state, and then the voltage across the junction of the transistor Q_1 is noted.
6. The output waveforms are plotted for V_{C1} , V_{B1} , V_{C2} , V_{B2} which are observed from the CRO.

RESULT:

A monostable multivibrator is studied and output wave forms were verified.

Exp No: 10 **Date:**

BISTABLE MULTIVIBRATOR

AIM:

To conduct and verify the Bistable multivibrator and draw the waveforms.

COMPONENTS REQUIRED:

1. Transistor BC 547 ---------- 2 No's
2. Capacitor 100PF, 0.01 μF ------ 1 No each
3. Resistors 680 Ω ---------- 2 No's
   10 KΩ ---------- 2 No's
   15 KΩ ---------- 2 No's
   220 KΩ ---------- 2 No's
4. Diode IN 4007 ---------- 2 No's
5. Bread Board
6. Connecting wires as required
7. CRO & Probes
8. Function Generator
9. Regulated Power Supply (0 - 30V)

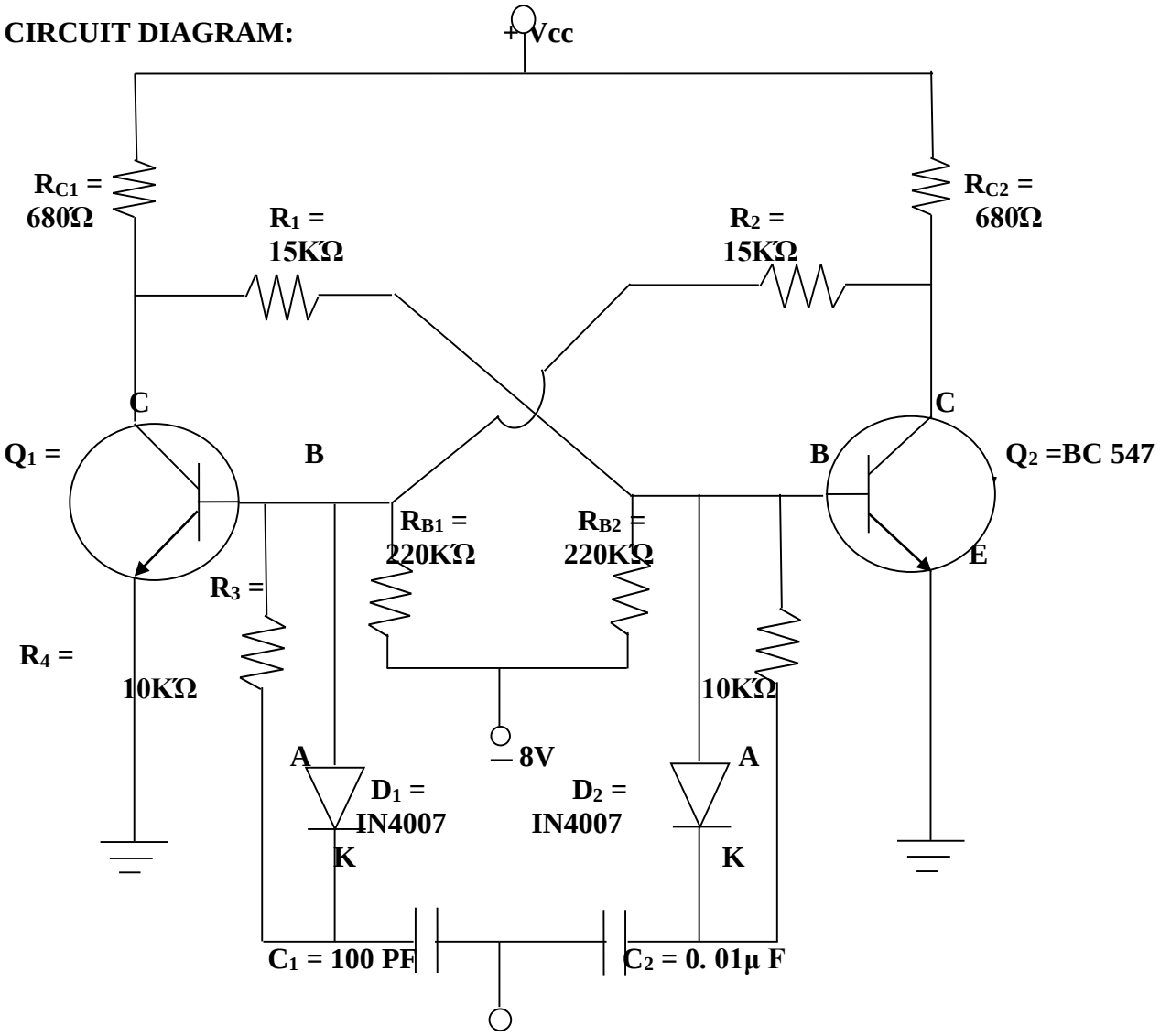
THEORY:

A Bistable multivibrator has two stable output states. It can remain indefinitely in any one of the two stable states and it can be indeed to make abrupt transistion to the other stable state by means of suitable external exitation.

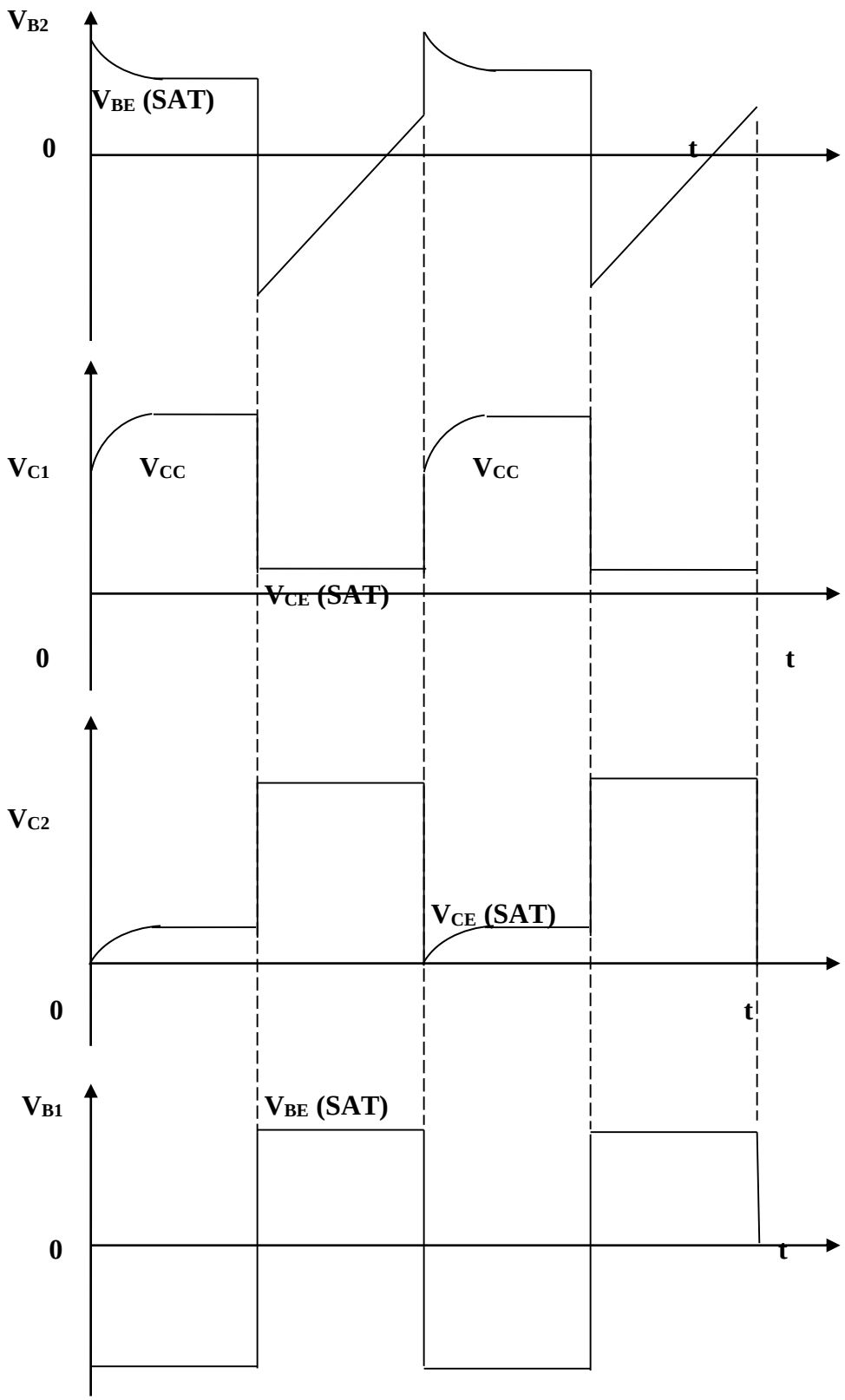
It would remain indefinitely in their stable state by external triggering.

Bistable multivibrators are also tuned as binaries or flip-flops. A binary is sometimes referred to as cutter-Jordan circuit. The transistors are identical: their quiescent currents would be the same unless the loop gain is greater than unity.

CIRCUIT DIAGRAM:



MODEL GRAPH:


V_{B2}
V_{BE} (SAT)
0
t
V_{C1}
V_{CC}
V_{CC}
V_{CE} (SAT)
0
t
V_{C2}
V_{CE} (SAT)
0
t
V_{B1}
V_{BE} (SAT)
0
t

V_{B2} = Voltage at base of Q_2
V_{C1} = Voltage at collector of Q_1
V_{C2} = Voltage at collector of Q_2
V_{B1} = Voltage at base of Q_1

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. An external triggering signal across the cathode terminal of the diode was applied.
3. The output voltage V_{C2} across the collector Q_2 considering that Q_1 is off and Q_2 is on was taken.
4. The output voltage V_{B2} across the base of transistor Q_2 was collected.
5. The above steps were repeated for Q_1 is on and Q_2 is off.
6. The output waveforms from the CRO was noted down and the graph was plotted

RESULT:

A Bistable multivibrator is studied and output wave forms are verified.

Exp No: 11 **Date:**

SCHMITT TRIGGER

AIM:

To construct and study the characteristics of Schmitt Trigger.

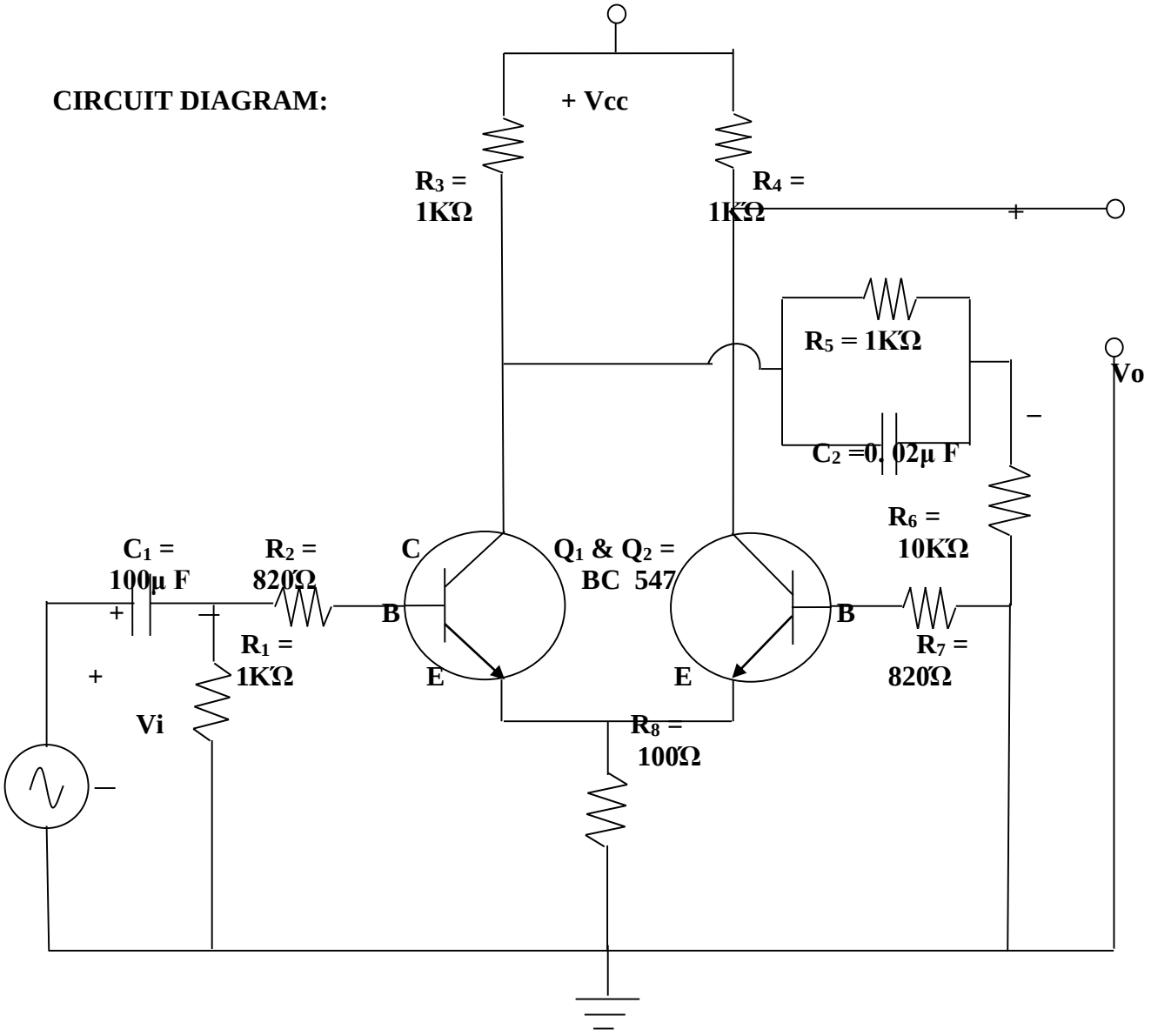
COMPONENTS REQUIRED:

1. Transistor BC 547 ---------- 2 No's
2. Capacitor 100 μF, 0.01 μF ------ 1 No each
3. Resistors 100 Ω ---------- 1 No
   820 KΩ ---------- 2 No's
   1 KΩ ---------- 4 No's
   10 KΩ ---------- 1 No
4. Bread Board
5. Connecting wires as required
6. CRO & Probes
7. Function Generator
8. Regulated Power Supply (0 - 30V)

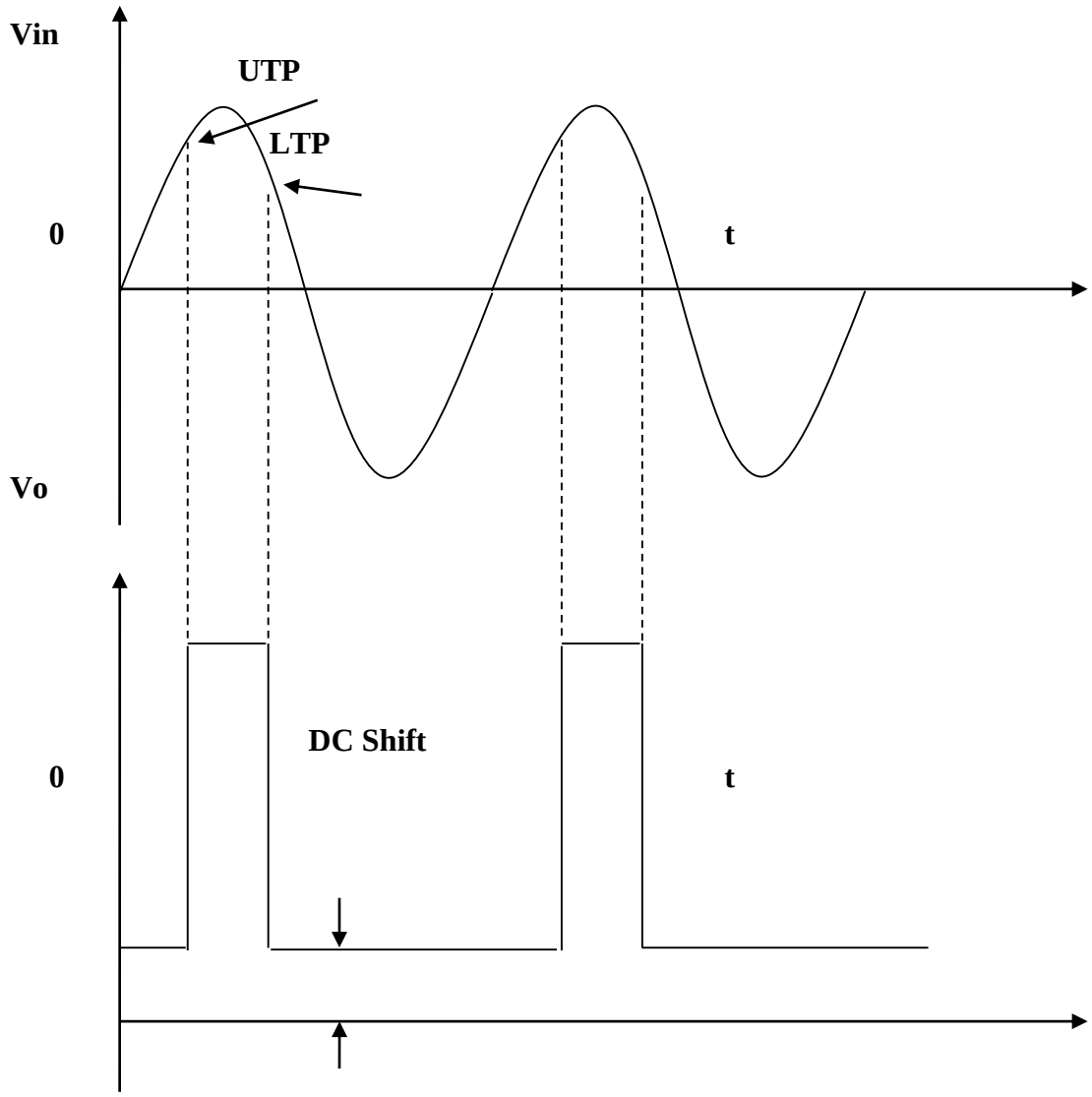
THEORY:

Schmitt trigger is a special type of Bistable multivibrator in which it differs from basic binary circuit in that resistive coupling between the output of Q_2 and the input of Q_1 of the basic circuit is missing, although the collector of Q_1 and the base of Q_2 are coupled. Therefore Schmitt trigger can also be called as Emitter coupled binary. The emitters of Q_1 & Q_2 are joined and they are grounded through a common resistor R_E . The input voltage source V_i is given to the base of Q_1 . The value of input voltage which makes Q_1 conduct is termed as Upper triggering point or Upper trip point (UTP). Similarly the value of input voltage which makes Q_2 conduct again is termed as Lower triggering point or Lower trip point (LTP).

CIRCUIT DIAGRAM:



MODEL GRAPH:



The values of UTP & LTP is given by

$$UTP = V_{\gamma} + i_{C2} R_E \quad \text{and}$$

$$LTP = V_{BE\,(ACTIVE)} + i_{C2} R_E$$

PROCEDURE:

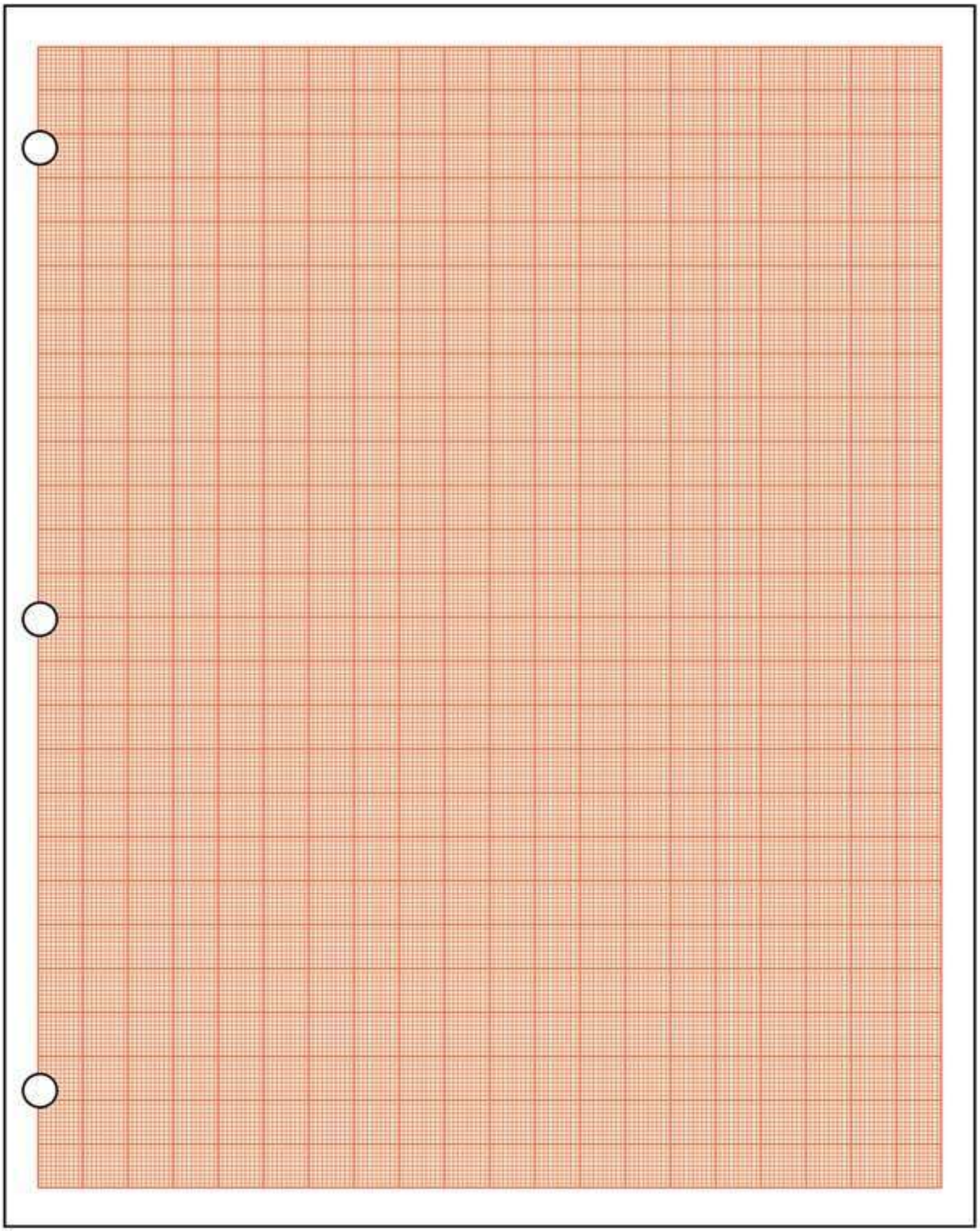
1. Connect the circuit as shown in the circuit diagram.
2. Apply the voltage V_{CC} = 12V.
3. A sine wave of amplitude 10V is applied as an input to the circuit through the base of Q_1.
4. The values of UTP and LTP were noted down from the waveforms obtained from the CRO and the graph was plotted.

RESULT:

Thus the Schmitt Trigger circuit was constructed and UTP, LTP values were noted.

UTP = _____ V

LTP = _____ V



Exp No: 12 **Date:**

UJT RELAXATION OSCILLATOR

AIM:

To construct and verify the UJT Relaxation Oscillator and its output waveform.

COMPONENTS REQUIRED:

1. UJT 2N2426 ---------- 2 No's
2. Capacitor 200 PF ---------- 1 No
3. Resistors 47 Ω ---------- 1 No
   680 Ω ---------- 2 No
   56 KΩ ---------- 4 No
4. Bread Board
5. Connecting wires as required
6. CRO & Probes
7. Regulated Power Supply (0 - 30V)

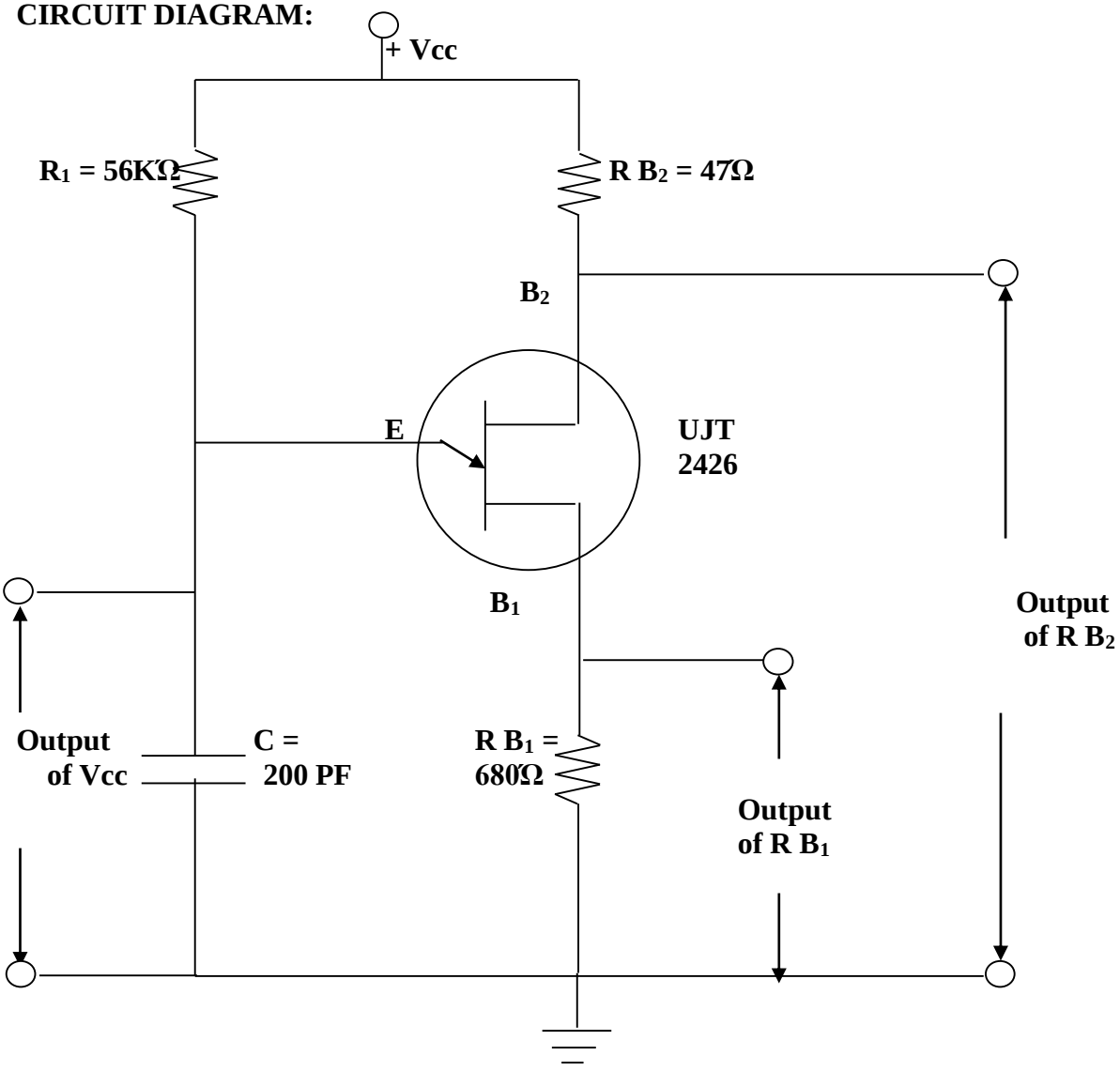
THEORY:

The UJT Sweep circuit is as shown in diagram. We studied that a UJT is off as long as VE, VR1 the peak voltage. Hence initially when UJT is OFF the capacitor "C" charges through resistor from the supply.

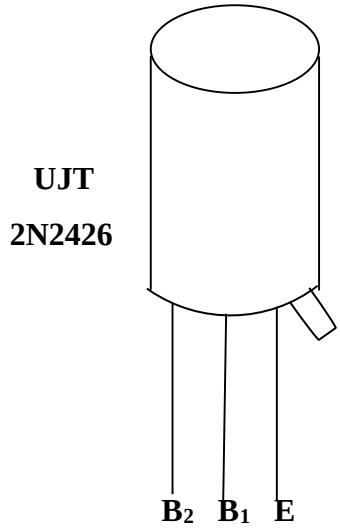
It is seen that when capacitor voltage rises to a certain value the UJT readily conducted when UJT raises on the capacitor discharges and its voltage falls. When voltage falls to the valley point the UJT becomes off the capacitor charges again to Vp.

The cycle of charging and discharging of the capacitor repeat and as a result a saw tooth wave form of voltage across "C" is generated.

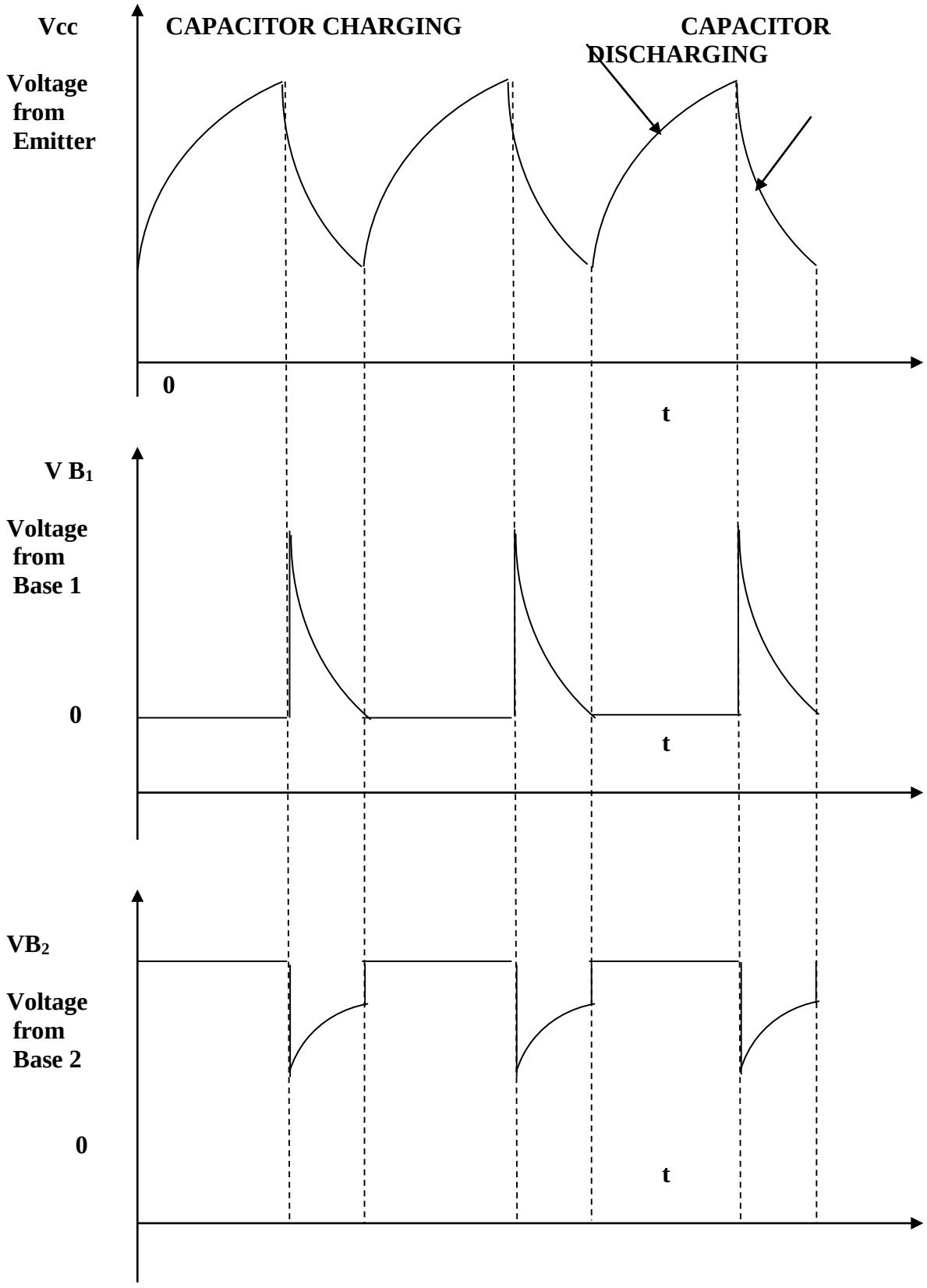
CIRCUIT DIAGRAM:



UJT PIN DETAILS:



MODEL GRAPH:


Vcc
CAPACITOR CHARGING
CAPACITOR DISCHARGING
Voltage from Emitter
0
t
V B1
Voltage from Base 1
0
t
VB2
Voltage from Base 2
0
t

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Apply the voltage V_{CC} = 12V.
3. The output wave forms of emitter, base1 and base2 are noted from the CRO and the graph were plotted.

RESULT:

The UJT relaxation Oscillator was constructed and the output wave forms are verified.