Exp. No. : **Date:**

AMPLITUDE MODULATION AND DEMODULATION

AIM

To verify amplitude modulation and demodulation and to calculate the modulation index of an AM modulated wave

EQUIPMENTS:

- Modules ACL-AM & ACL-AD.
- Power supply
- 20MHz Oscilloscope.
- Connecting Links.
- Frequency counter

THEORY

In Amplitude Modulation the amplitude of high frequency sine wave (carrier) is varied in accordance with the instantaneous value of the modulating signal.

Consider a sine signal $v_m(t)$ with frequency f

$V_m(t) = B \bullet \text{Sin}(2\pi f \bullet t)$

And another sine signal $V_c(t)$ is called modulating signal, the signal $V_c(t)$ is called carrier signal.

$V_c(t) = A \bullet \text{Sin}(2\pi F \bullet t)$

The signal $V_m(t)$ is called modulating signal; the signal $V_c(t)$ is called carrier signal.

Vary the amplitude of the carrier vc(t) adding the modulating signal vm(t) to A. You obtain a signal vM(t) amplitude modulated, which can be expressed by:

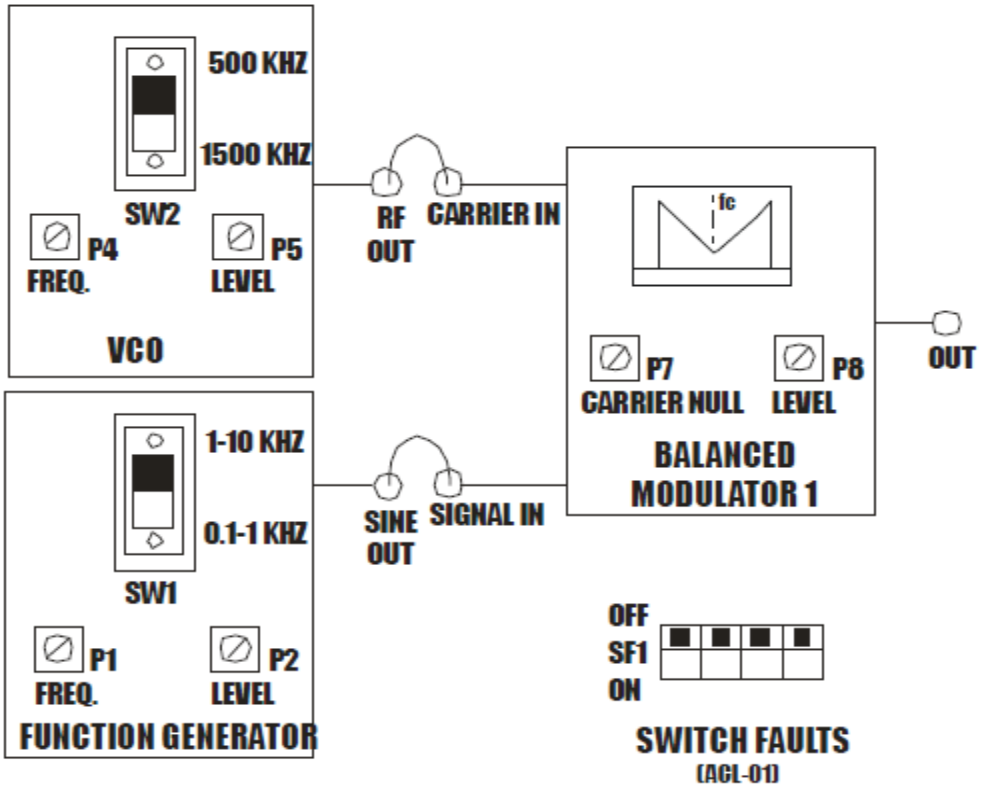
$V\,m(t) = [A+k \bullet B \bullet \sin(2\pi f \bullet t)] \bullet \sin(2\pi F \bullet t) = A \bullet [1+m \bullet \sin(2\pi f \bullet t)] \bullet \sin(2\pi F \bullet t)$

With k = constant of proportionality

The modulation index m can be calculated in this way

$$m = \frac{H-h}{H+h} \cdot 100\%$$

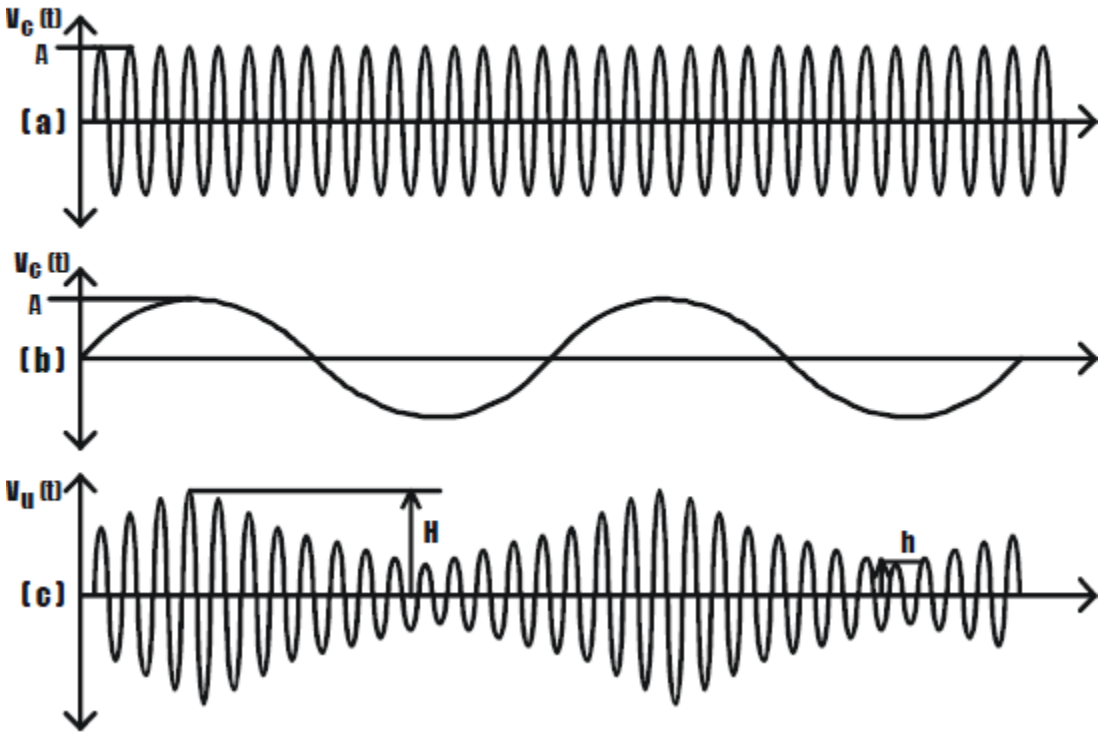
BLOCK DIAGRAM FOR AM MODULATION



PROCEDURE:

1. Connect **SINE OUT** post of **FUNCTION GENERATOR** SECTION (ACL-AM) to the i/p of Balance Modulator1 (ACL-AM) **SIGNAL IN** Post.
2. Connect o/p of **VCO** (ACL-AM) **RF OUT** post to the input of Balancemodulator1 **CARRIER IN** post (ACL-AM).
3. Connect the power supply with proper polarity to the kit ACL-AM & ACL-AD, while connecting this; ensure that the power supply is OFF.
4. Switch on the power supply and Carry out the following presetting:
   FUNCTION GENERATOR: LEVEL about 0.5Vpp; FREQ. about 1 KHz.
   VCO: LEVEL about 1 Vpp; FREQ. about 450 KHz, Switch on 500KHz
   BALANCED MODULATOR1: CARRIER NULL completely rotated
   Clockwise or counter clockwise, so as to "unbalance" the modulatorand to obtain an AM signal with not suppressed carrier across theoutput; OUT LEVEL in fully clockwise.
5. Connect the oscilloscope to the inputs of the modulator post (SIG and CAR) and detect the modulating signal and the carrier signal
6. Move the probe from post SIG to post OUT (output of the modulator), where signal modulated in amplitude is detected .
   Note that the modulated signal envelope corresponds to the wave form of the DSB AM modulating signal.
7. Vary the frequency and amplitude of the modulating signal, and check the corresponding variations of the modulated signal.
9. Vary the amplitude of the modulating signal and note that the modulated signal can result saturation or over modulation.

MODEL WAVE FORMS



DEMODULATION:

PROCEDURE:

1. Refer to the FIG. 2.8 & Carry out the following connections.

2. Connect o/p of **FUNCTION GENERATOR** section (ACL-AM) **OUT** post to the i/p of Balance Modulator1 (ACL-AM) **SIGNAL IN** post.

3. Connect o/p of VCO (ACL-AM) **OUT** post to the input of Balance modulator 1 (ACL-AM) **CARRIER IN** post.

4. Connect the power supply with proper polarity to the kit ACL-AM & ACL -AD, While connecting this, ensure that the power supply is OFF.

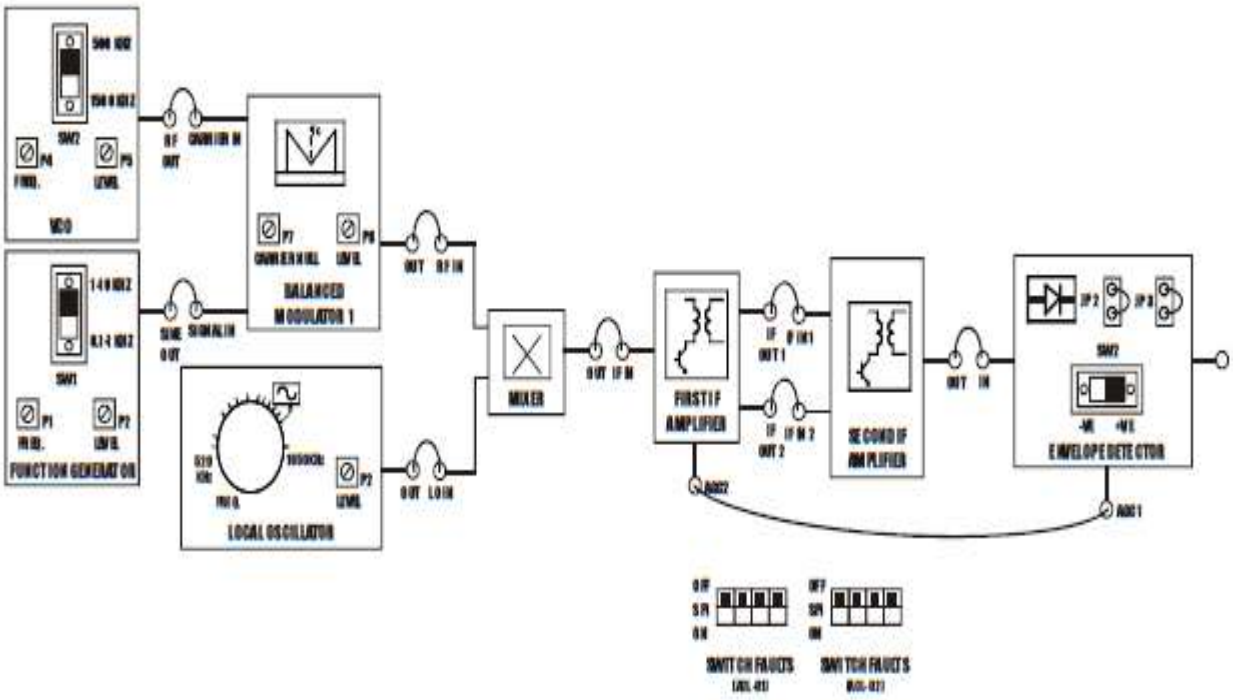
5. Switch on the power supply and Carry out the following presetting:

• **FUNCTION GENERATOR:** Sine LEVEL about 0.5 Vpp; FREQ. about 1 KHz.

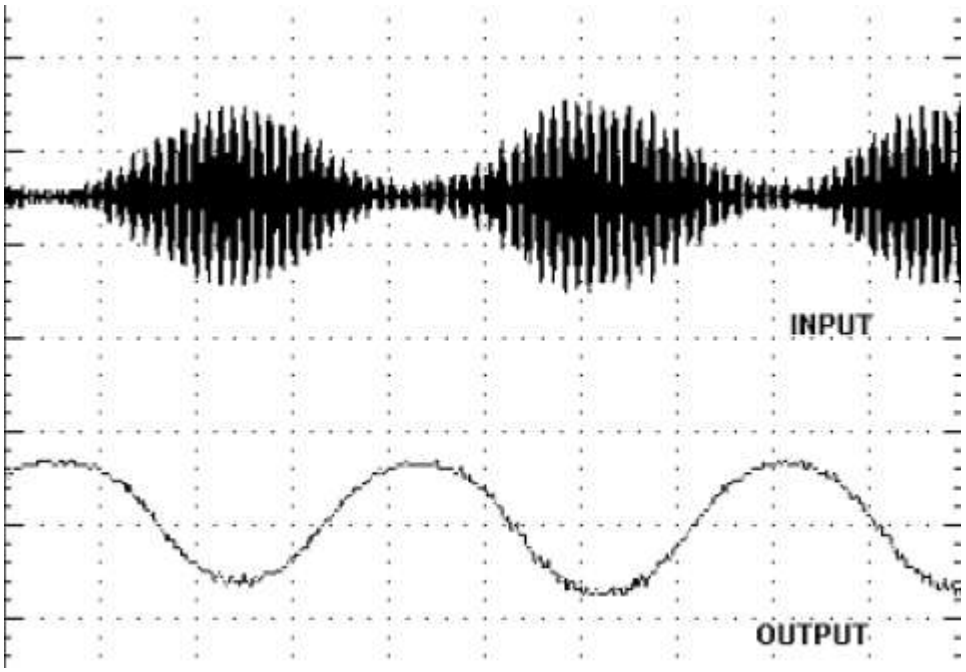
• **VCO:** LEVEL about 2Vpp; FREQ. about 850 KHz, Switch on 1500KHz.

• **BALANCED MODULATOR1:** CARRIER NULL completely rotates Clockwise or counter clockwise, so that the modulator is "unbalanced" and an AM signal with not suppressed carrier is obtained across the output: adjust OUTLEVEL to obtain an AM signal across the output whose amplitude is about 100mVpp

• **LOCAL OSCILLATOR (ACL-AD):** 1300KHz, 2V.



MODEL WAVE FORMS



Result

Exp. No. : **Date:**

FREQUENCY MODULATION AND DEMODULATION

AIM

To verify Frequency Modulation and Demodulation

To measure frequency deviation and modulation index of FM.

EQUIPMENTS

ACL-FM & ACL-FD Kits.

Power supply.

Oscilloscope.

Volt meter.

Frequency meter.

Connecting Links.

THEORY

It is a type of modulation in which the frequency of the high frequency (Carrier) isvaried in accordance with the instantaneous value of the modulating signal.

Consider a sine wave signal vm(t) with pulse w

vm(t) = B • sin(w•t)

and another sine wave vc(t) with upper Ω pulse:

vc(t) = A • sin(Ω•t)

The signal vm(t) is called modulating signal, the signal vc(t) is called carrier signal.Vary the frequency of the carrier vc(t) in a way proportional to the amplitude of the modulating signal vm(t). You obtain a vm(t) frequency modulated diagonal, which canbe expressed by the relation:**vm(t) = A • sin [θ(t)]**

with**θ**(t) instantaneous angle function of vm(t).

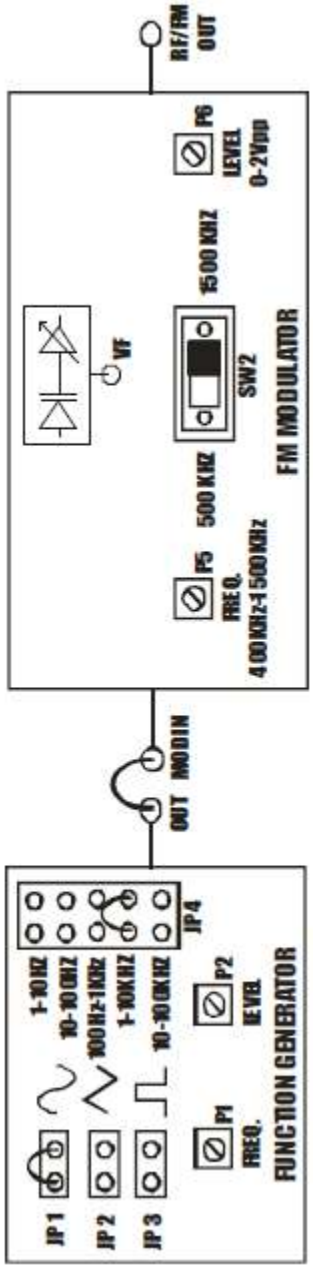
The instantaneous pulse F(t) of the FM signal by definition:

Ω(t) = Ω+ K• vm(t)

The frequency deviation ΔF represents the maximum shift between the modulatedsignal frequency, over and under the frequency of the carrier:**ΔF =** $\frac{F_{max}-F_{min}}{2}$

We define as modulation index mf the ratio between **ΔF** and the modulating frequency f:$mf = \frac{\Delta F}{f}$

BLOCK DIAGRAM



PROCEDURE

1. Connect the power supply with proper polarity to the kit ACL-FM while connecting this; ensure that the power supply is OFF.

2. Connect the o/p of function generator **OUT** post to the modulation **IN** of FREQUENCY MODULATOR **MOD IN** post.

3. Switch ON the power supply and Carry out the following presetting:-

FUNCTION GENERATOR: sine wave (JP1); LEVEL about 100mV;FREQ**.** about 1KHz.

- **FREQUENCY MODULATOR** LEVEL about 2Vpp; FREQ**.** on thecenter; switch on 1500KHz.

4.Connect the oscilloscope to the output of the modulator FM/RF OUT.

5.The frequency deviation _ F can be calculated as follows

- From the oscilloscope evaluate FM and Fm, detecting the periods of the respective sine waves

- The frequency deviation $\Delta\mathbf{F}$ is defined as: $\Delta\mathbf{F} = (FM - Fm)/2$

You can note that if the modulator operates in a linear zone so FM and Fm are over and under the central frequency F of the same quantity $\Delta\mathbf{F}$, otherwise this does not occur.

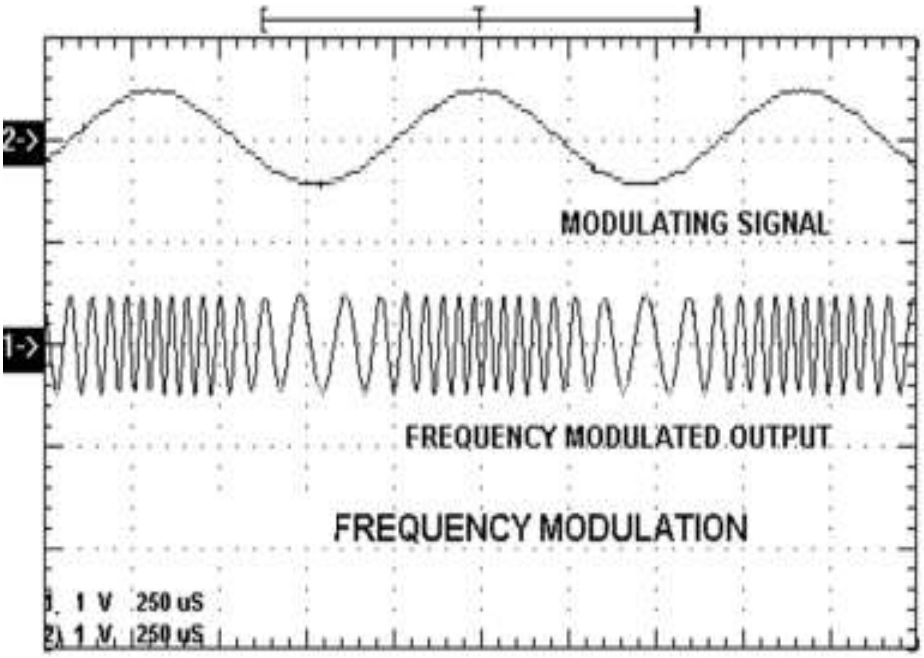
6.The value of the modulation index mf is calculated by the relation

mf = $\Delta\mathbf{F}/f$, where f is the frequency of the modulating signal.

7.Then observe the FM signal as shown in FIG.

8.To observe the FM at lower frequencies apply Sine wave of 1KHz and 1Vpp from external function generator to **MOD IN** post of onboard Function Generator and keep JP4 at 10-100KHz position and adjust the frequency at about 20-25KHz and output level of Function generator at 2Vpp.

MODEL WAVE FORMS



DEMODULATION

PROCEDURE

1.Connect the o/p of Function Generator (ACL-FM) **OUT** post to the **MOD IN**(ACL-FM) post.

2.Connect the o/p of FREQUENCY MODULATOR **FM/RF OUT** post to the I/p ofRF IN of mixer

3.Connect the power supply with proper polarity to the kit ACL-FM & ACL-FD,while connecting this; ensure that the power supply is OFF.

4.Switch ON the power supply and Carry out the following presetting:

- **Frequency Modulator:** Switch on 500KHz; LEVEL about 1 Vpp;FREQ. about 450 KHz.
- Frequency demodulator in Foster-Seeley mode (jumpers in FSposition).
- **Function Generator:** Sine wave (JP1); LEVEL about 100mVpp;FREQ. about 1 KHz.
- **Local Oscillator:** LEVEL about 1 Vpp; FREQ. About1000 KHz on(Center).

5. Connect the LOCAL OSCILLATOR **OUT** to the **LO IN** of the MIXER and MIXER **OUT** to the LIMITER **IN** post with the help of shorting links.

Then connect the LIMITER **OUT** post to the **FM IN** of FOSTER- SEELEY DETECTOR and **FS OUT** to the **IN** of LOW PASS FILTER.

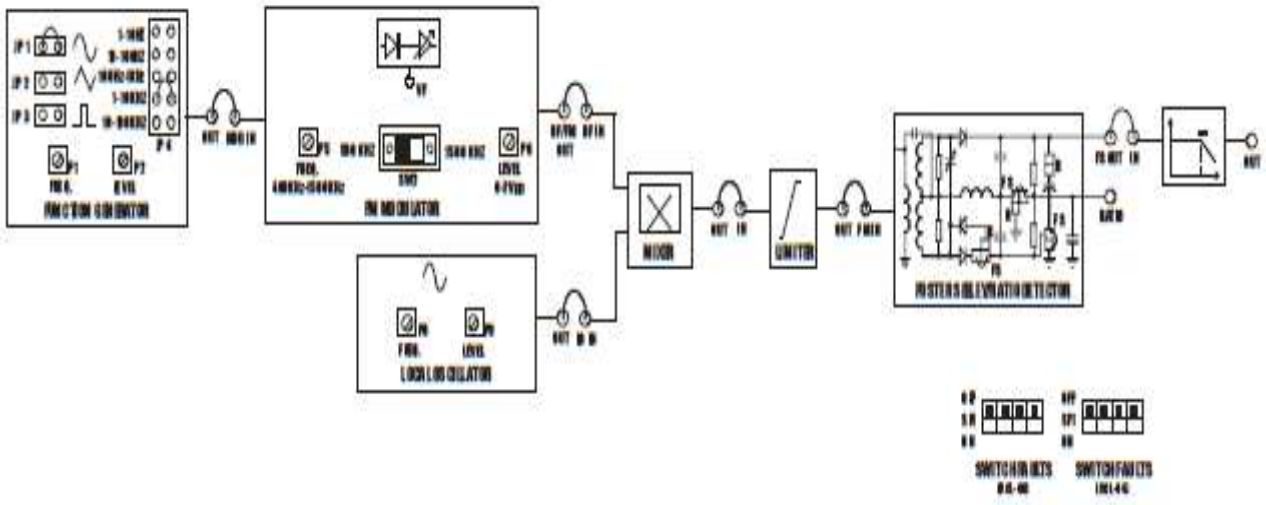
7. Then observe frequency modulated signal at FM/RF **OUT** post of FREQUENCY MODULATOR and achieve the same signal by settingfrequency of LOCAL OSCILLATOR at **OUT** post of **MIXER,** then observe LIMITER OUT post where output is clear from noise and stabilize around a value of about 1.5Vpp.

8. Connect the oscilloscope across post **FS OUT** of ACL-FD (detected signal) and FUNCTION GENERATOR **OUT** post (modulating signal) of ACL-FD. If the central frequency of the discriminator and the carrier frequency of the FM signal and local oscillator frequency coincide, you obtain two signals The fact that there is still some high-frequency ripple at the output of the FOSTERSEELEY DETECTOR block indicates that the passive low pass filter circuit atthe block's output is not sufficient to remove this unwanted high-frequency component. We use the LOW PASS FILTER block to overcome this problem. The LOW - PASS FILTER block strongly attenuates the high-frequency ripple component at the detector's output, and also blocks the d.c. offset voltage. Consequently, the signal at the output of the LOW - PASS FILTER block should very closely resemble the original audio modulating signal.

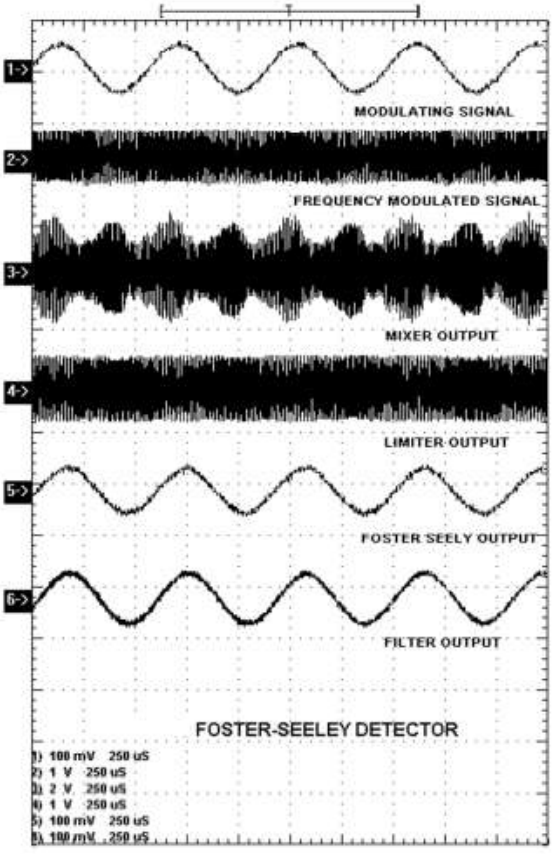
9. Note that the demodulated signal has null continuous component. Vary the amplitude of the FM signal and check that the amplitude of the detected signal varies, too.

10. Increase the carrier frequency and note that a positive voltage is added to the detected signal. Still increasing the frequency, the detected signal presents a distortion

BLOCK DIAGRAM



MODEL WAVEFORMS



RESULT:

Exp. No. : **Date:**

PRE-EMPHASIS AND DE-EMPHASIS

AIM

To verify Pre-Emphasis and De- emphasis Circuit and it's Response

EQUIPMENTS

- ACL-FM & ACL-FD Kits
- Power supply
- Oscilloscope
- Frequency meter
- Connecting links

THEORY

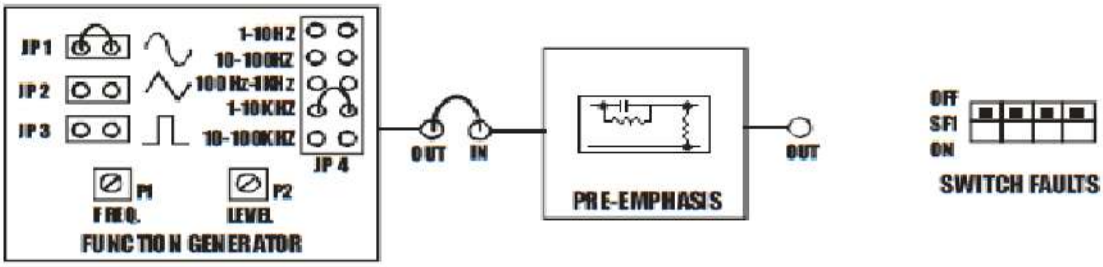
Need For Pre Emphasis

Frequencies contain in human speech mostly occupy the region from 100 to 10,000 Hz, but most of the power is contained in the region of 500 Hz for men and 800 Hzfor women. Common voice characteristics emit low frequencies higher in amplitudethan higher frequencies. The problem is that in FM system the noise output of thereceiver increases linearly with the frequency, which means that the signal to noiseratio becomes poorer as the modulating frequency increases.Also, noise can make radio reception less readable and unpleasant. This noise isgreatest in frequencies above 3KHz.The high frequency noise causes interference tothe already weak high frequency voice. To reduce the effect of this noise and ensurean even power spread of audio frequencies,

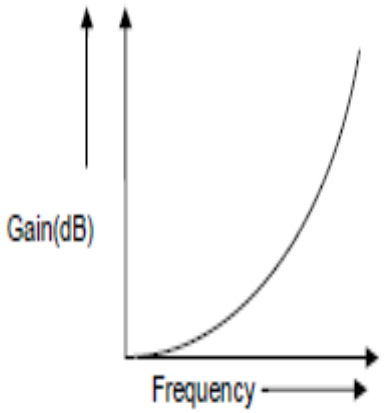
Pre emphasis is used at the Transmitter Side

A pre-emphasis network in the transmitter accentuates the audio frequencies above3 KHz, so providing the higher average deviation across the voice spectrum, thusimproving the signal to noise ratio.The pre-emphasis is obtained by using the simple audio filter, even simple RC filterwill do the job. The pre-emphasis circuit produces higher output at higherfrequencies because the capacitive reactance is decreased as the frequencyincreases.

BLOCK DIAGRAM



MODEL WAVE FORM



PROCEDURE:

The characteristic of pre-emphasis circuit is given by output voltage of the preemphasis circuit as the function of instantaneous input frequency. It is possible toplot the curve of fig. By varying the input frequency and measuring thecorresponding output voltage.

1 Make the connections as shown in the block diagram Fig.2.1.

2.Connect the power supply with proper polarity to the kit ACL-FM while

connecting this; ensure that the power supply is OFF.

3. Connect the output of function generator to the IN of pre-emphasis circuit.

4. Switch on the power supply and carry out the following presetting.

5.FUNCTION GENERATOR: Frequency about 1KHz and level of 100mV p-psine wave

Now vary the frequency in steps of 500Hz and note down the output voltageat the OUT post of pre-emphasis circuit.

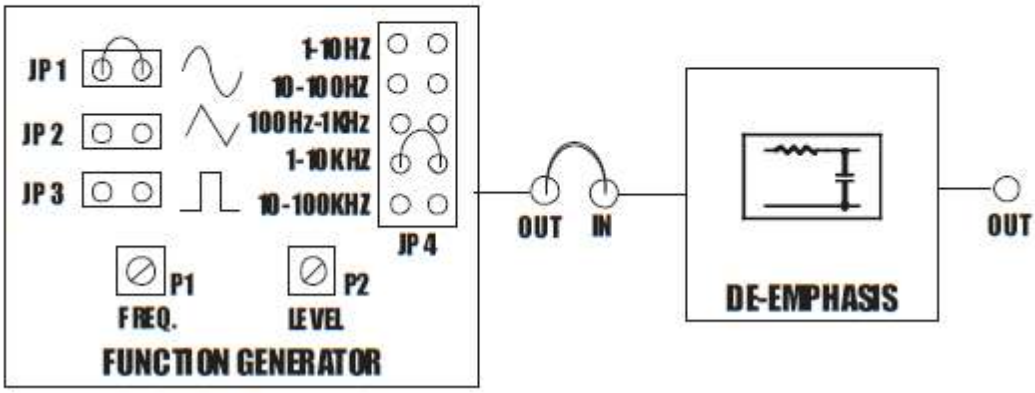
6. Plot the graph of output voltage v/s input frequency on graph paper. Theresponse should come as shown in the theory above.

7. From the response you can easily understand that using the pre-emphasisCircuit we can increase the amplitude of modulating signal at higherfrequencies thus improving the Signal to Noise ratio at higher frequencies of the pre-emphasis.

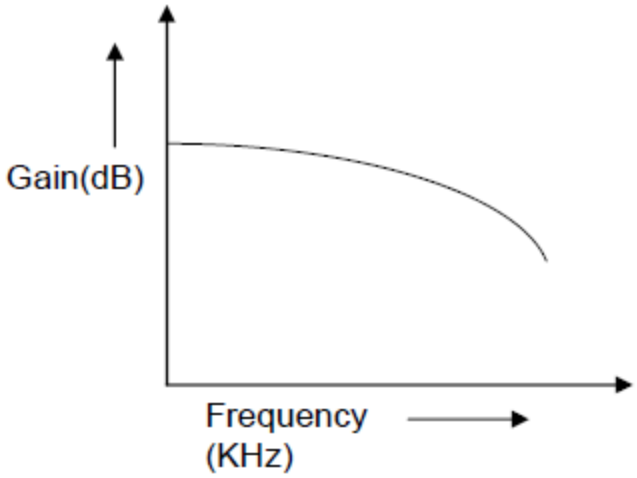
De emphasis:

The problem in FM broadcasting is that noise and hiss tends to be more noticeable,especially when receiving the weaker stations .To reduce this effect, the trebleresponse of the audio signal is artificially boosted prior to transmission. This isknown as pre emphasis.At the receiver side a corresponding filter or “de emphasis” circuit is required toreduce the treble response to correct level. Since most noise and hiss tends to be atthe higher frequencies , the de emphasis removes a lot of this. Pre emphasis and deemphasis thus allow an improved signal to noise ratio to be achieved whilemaintaining the frequency response of the original audio signal.The de emphasis stage is used after the detector stage.The response of the de emphasis circuit can be understood from the following graph:

BLOCK DIAGRAM



MODEL WAVEFORM



PROCEDURE

The characteristic of de-emphasis circuit is given by output voltage of thedeemphasize circuit as the function of instantaneous input frequency. It is possible toplot the curve of fig. By varying the input frequency and measuring thecorresponding output voltage.

1. Make the connections as shown in the block diagram .
2. Connect the power supply with proper polarity to the kit ACL-FD whileconnecting this; ensure that the power supply is OFF.
3. Connect the output of function generator(ACL-FM) to the IN of de-emphasis' circuit(ACL-FD).
4. Switch on the power supply and carry out the following presetting.
5.FUNCTION GENERATOR: Frequency about 1KHz and level of 100mV p-p sine wave
6. Now vary the frequency in steps of 500Hz and note down the output voltage at the OUT post of de-emphasis circuit.
7. Plot the graph of input frequency v/s output voltage on graph paper. The response should come as shown in theory.

RESULT

Exp. No. : **Date:**

PULSE AMPLITUDE MODULATION AND DE MODULATION

AIM:

To verify Pulse Amplitude Modulation. And Demodulation

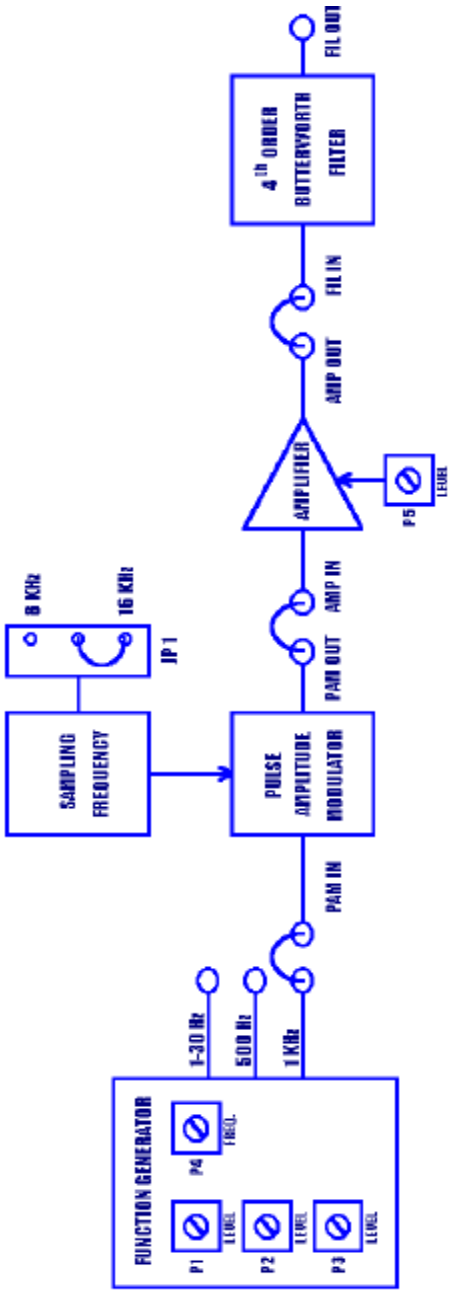
EQUIPMENTS

Experimenter kit DCL-08.
Connecting Chords
Power supply
20 MHz Dual trace oscilloscope

THEORY:

In Pulse Amplitude Modulation, the signal is sampled at regular intervals and the amplitude of each sample is made proportional to the amplitude of the signal at that instant of sampling. This amplitude of each sample is hold for the sample duration to make pulses flat top. The Pulse Amplitude Demodulator consists of Active Low Pass Butterworth filter. It filters out the sampling frequency and their harmonics from the modulated signal and recovers the base band by integrated action.

BLOCK DIAGRAM

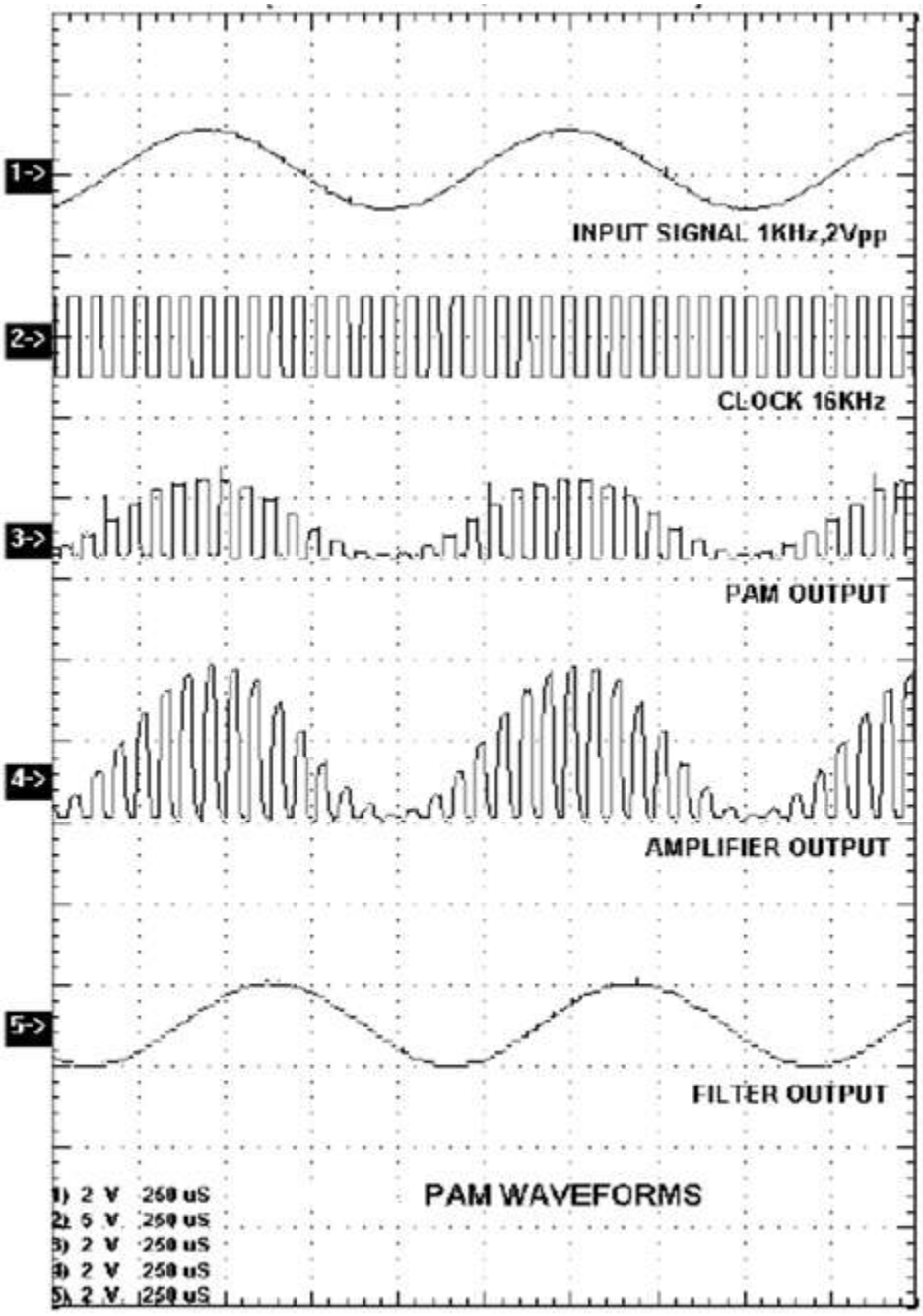


PROCEDURE

1.Connect the Power Supply with proper polarity to the kit **DCL-08** and switch it on.
2.Select **16 KHz** sampling frequency by jumper **JP1**.
3.Connect the **1 KHz**, 2Vp-p sine wave signal generated onboard to **PAM IN** Post.
4.Observe the Pulse Amplitude Modulation output at **PAM OUT** Post.
5.Short the following posts with the Connecting chords provided as shown in block diagram.
PAM OUT and **AMP IN**
AMP OUT and **FIL IN**

6.Keep the amplifier gain control potentiometer **P5** to maximum completely clockwise.
7.Observe the Pulse Amplitude Demodulated signal at **FIL OUT**, which is same as the input signal.
8. Repeat the experiment for different input signal and sampling frequencies

MODEL WAVE FORMS



RESULT

Exp. No. : **Date:**

PULSE WIDTH MODULATION AND DEMODULATION

AIM

To verify Pulse Width Modulation and Demodulation

EQUIPMENTS

Experimenter kit DCL-08.

Connecting Chords

Power supply

20 MHz Dual trace oscilloscope

THEORY

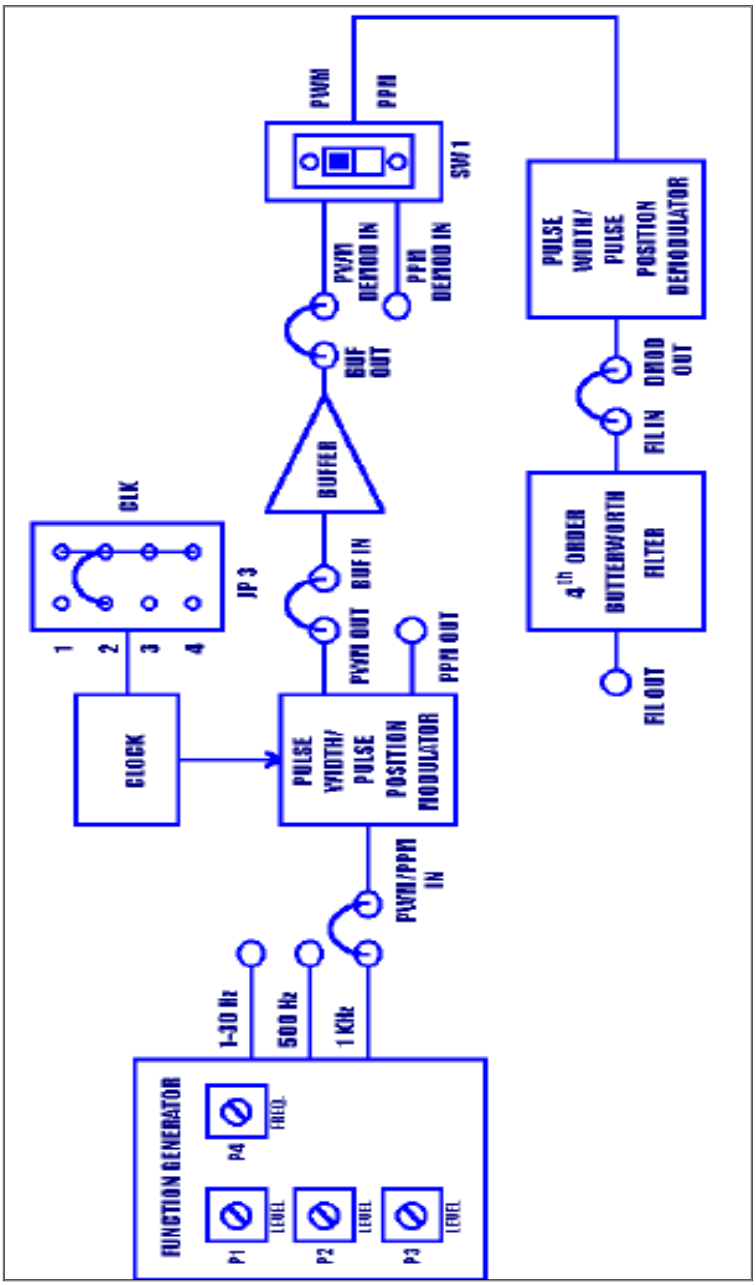
Pulse Width Modulation

This technique of modulation controls the variation of duty cycle of the square wave (With some fundamental frequency) according to the input modulating signal. Here the amplitude variation of the modulation signal is reflected in the ON period variation of square wave. Hence, it is a technique of V to T conversion.

Pulse Width Demodulation

The input signal is Pulse Width Modulated, so the ON time of the signal is changing according to the modulating signal. In this demodulation technique during the ON time of PWM signal one counter is enabled. At the end of ON time, counter gives a particular count, which directly corresponds to the amplitude of input signal. Then this count is fed to a DAC. The output of DAC corresponds to the amplitude of input signal. Thus train of varying pulse widths gives varying count values and accordingly DAC give outputs, which is directly proportional to amplitude of input signal. This is then filtered to get original signal. Thus at the output we get the original modulating signal extracted from PWM wave.

BLOCK DIAGRAM



PROCEDURE

1. Connect the Power Supply with proper polarity to the kit **DCL-08** and switch it on.
DCL-08: PAM / PWM / PPM MODULATION & DEMODULATION KIT
2Put jumper **JP3** to 2nd position.
3. Select **1KHZ** 1v-pp sine wave signal generated onboard.
4. Connect this signal to **PWM/PPM IN**.

Observe the Pulse Width Modulated output at **PWM OUT** post. Note that since the sampling frequency is high, only blurred band in waveform will be observed due to persistence of vision. In absence of input signal only square wave of fundamental frequency and fixed on time will be observed and no width variation are present. To observe the variation in pulse width, apply 1-30Hz sine wave signal to **PWM/PPM IN** post. Vary the frequency from 1-30 Hz.

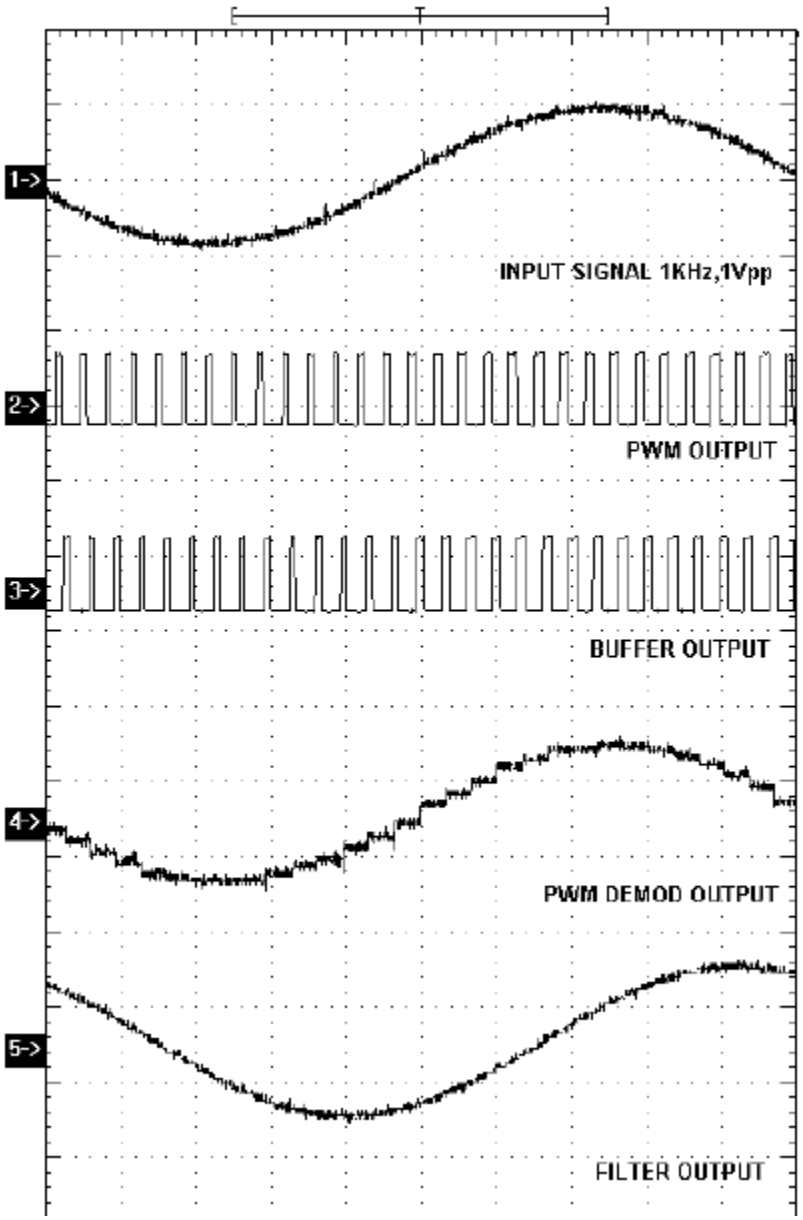
5.hort the following posts with the Connecting chords provided as shown in block diagram for demodulation section.

PWM OUT and **BUF IN**
BUF OUT and **PWM DMOD IN**
DMOD OUT and **FIL IN**

6. Observe the Pulse Width Demodulated output at **FIL OUT**.

7. Repeat the experiment for different input signal and different sampling clocks with the

MODEL WAVE FORMS



RESULT

Exp. No. : **Date:**

PULSE POSITION MODULATION AND DEMODULATION

AIM

To verify Pulse Position Modulation and Demodulation.

EQUIPMENTS

Experimenter kit DCL-08.

Connecting Chords

Power supply

20 MHz Dual trace oscilloscope

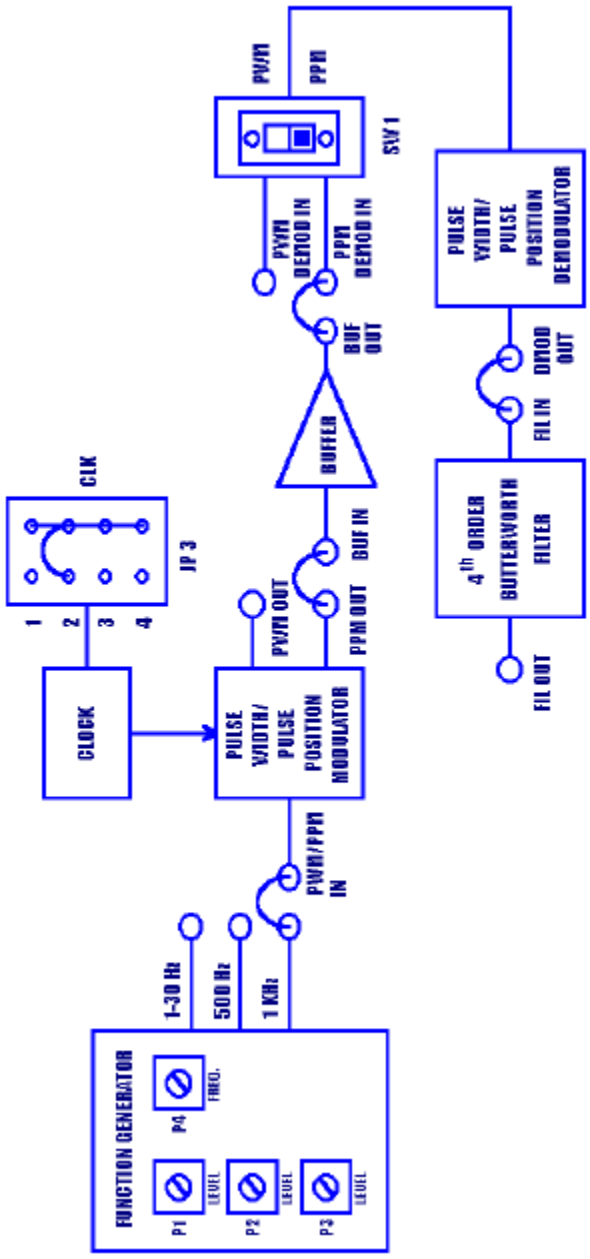
THEORY

The position of the TTL pulse is changed on time scale according to the variation of input modulating signal amplitude, Width of the pulses and Amplitude of the pulses remain same.

Demodulation

This pulse position modulated signal is converted into PWM pulse form using Monosatable multivibrator. This signal is then demodulated using the same technique of PWM demodulation. In this demodulation technique during the ON time of PWM signal one counter is enabled. At the end of ON time, counter gives a particular count, which directly corresponds to the amplitude of input signal. Then this count is fed to a DAC. The output of DAC corresponds to the amplitude of input signal. Thus train of varying pulse widths gives varying count values and accordingly DAC gives outputs, which is directly proportional to amplitude of input signal. This is then filtered to get original signal. Thus at the output we get the original modulating signal extracted from PWM wave

BLOCK DIAGRAM



PROCEDURE

1.Connect the Power Supply with proper polarity to the kit **DCL-08** and switch it on.

2.Put jumper **JP3** to 2nd position.

3.Select**1KHZ**, 1v-pp sine wave signal generated onboard.

4.Connect the selected signal to the **PWM/PPM IN.**

5.Observe the Pulse Position Modulated output at **PPM OUT** post with shifted position on time scale. Please note amplitude and width of pulse are same and there is shift in position which is proportional to input Analog signal.

6.To observe the variation in pulse positions, apply 1-30Hz sine wave signal to **PWM/PPM IN** post vary the frequency from 1-30 Hz and observe the signal on oscilloscope in dual for posts **PPM OUT** and **PWM OUT** simultaneously.

7.Then short the following posts with the link provided as shown in block diagram for Demodulation section.

PPM OUT and **BUFIN**

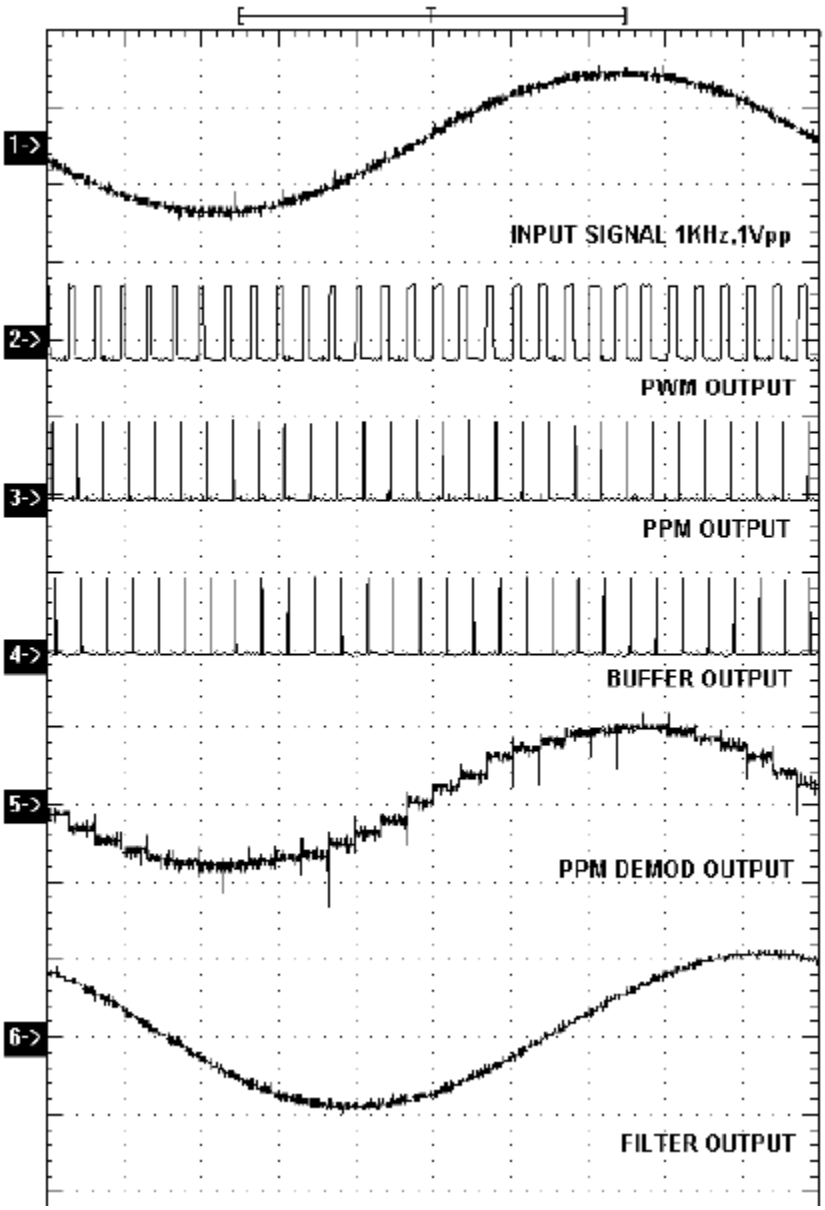
BUFOUT and **PPM DMOD IN**

DMOD OUT and **FIL IN**

8.Observe the Pulse Position Demodulated signal at **FIL OUT**.

9.Repeat the experiment at different input signal and different sampling frequencies.

MODEL WAVE FORMS



Result

Exp. No. : **Date:**

SAMPLING THEOREM – VERIFICATION

AIM

To verify sampling theorem.

EQUIPMENTS

- Experimenter kit DCL –01.
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

The kit is used to study Analog Signal Sampling and its Reconstruction. It basically consists of functional blocks, namely Function Generator, Sampling Control Logic, Clock section, Sampling Circuitry and Filter Section.

Function Generator

This Block generates two sine wave signals of 1 KHz and 2 KHz frequency. This sine wave generation is done by feeding 16 KHz and 32 KHz clock to the shift register. The serial to parallel shift register with the resistive ladder network at the output generates 1 KHz and 2 KHz sine waves respectively by the serial shift operation. The R-C active filter suppresses the ripple and smoothness the sine wave. The unity gain amplifier buffer takes care of the impedance matching between sine wave generation and sampling circuit.

Sampling Control Logic

This unit generates two main signals used in the study of Sampling Theorem, namely the analog signals (5V pp, frequency 1KHz and 2KHz) & sampling signal of frequency 2KHz, 4KHz, 8KHz, 16KHz, 32KHz, and 64KHz. The 6.4 MHz Crystal Oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies from 2 KHz to 64KHz and the other control frequencies.

From among the various available sampling frequencies, required sampling frequency is selected by using the Frequency selectable switch. The selected sampling frequency is indicated by means of corresponding LED.

BLOCK DIAGRAM

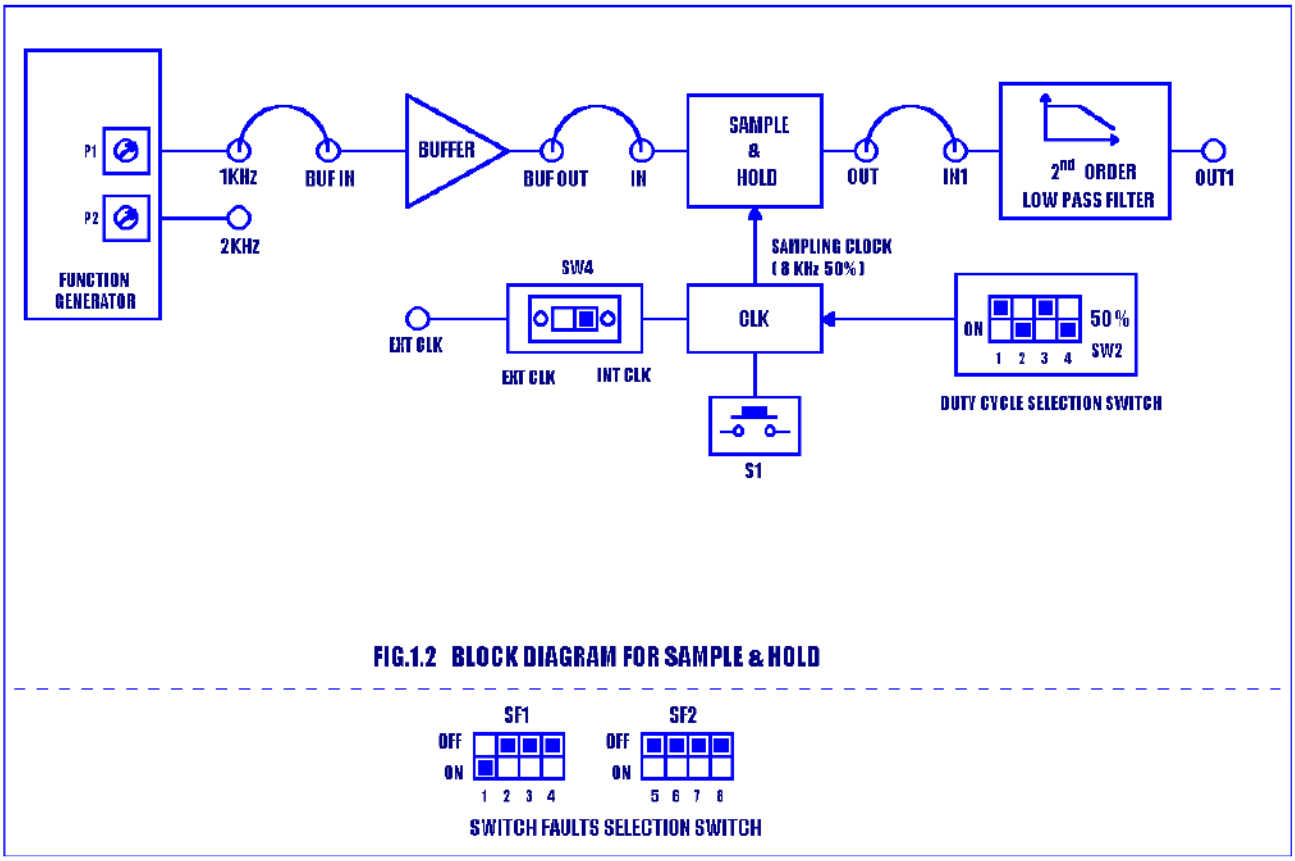


FIG.1.2 BLOCK DIAGRAM FOR SAMPLE & HOLD

Clock Section

This section facilitates the user to have his choice of external or internal clock feeding to the sampling section by using a switch (SW4).

Sampling Circuitry

The unit has three parts namely, Natural Sampling Circuit, Flat top Sampling Circuit, and Sample and Hold Circuit.

The Natural sampling section takes sine wave as analog input and samples the analog input at the rate equal to the sampling signal.

For sample and hold circuit, the output is taken across a capacitor, which holds the level of the samples until the next sample arrives. For flat top sampling clock used is inverted to that of sample & hold circuit. Output of flat top sampling circuit is pulses with flat top and top corresponds to the level of analog signal at the instant of rising edge of the clock signal.

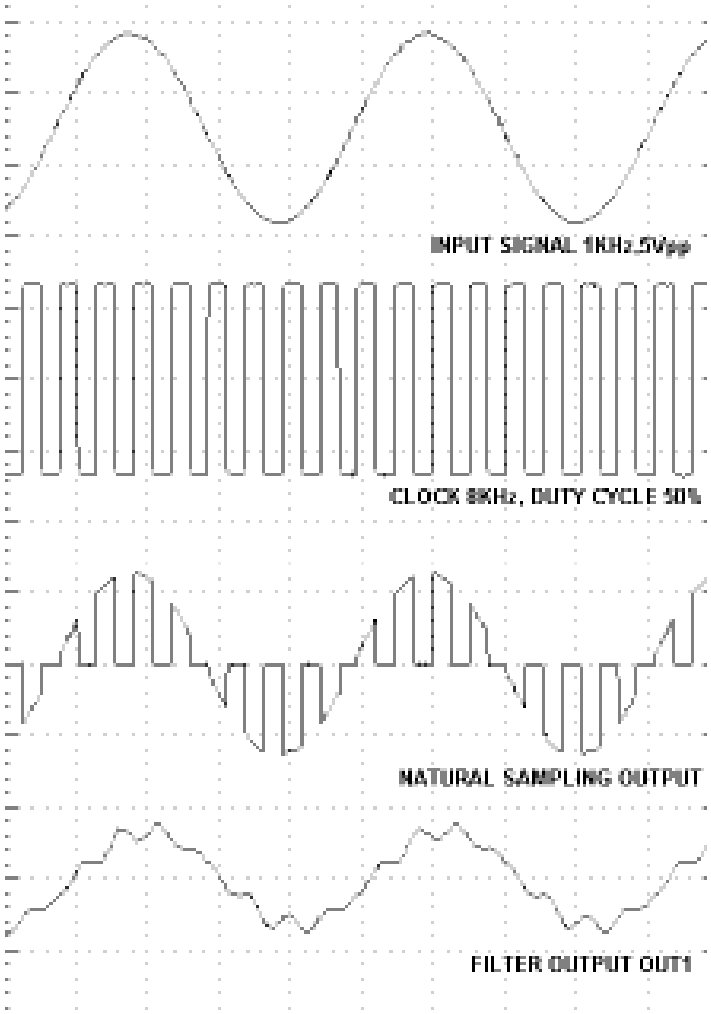
Filter Section

Two types of Filters are provided on board, viz., 2nd Order and 4th Order Low Pass Butterworth Filter.

PROCEDURE

1. Refer to the Block Diagram & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz**, 5Vpp Sine wave signal, generated on board, to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch **(SW4)**.
5. Using clock selector switch **(S1)** select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Natural sampling block to the input **IN1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below.
8. Repeat the procedure for the 2KHz sine wave signal as input.

MODEL WAVEFORMS



RESULT

Exp. No. : **Date:**

TIME DIVISION MULTIPLEXING

AIM

To verify Time Division Multiplexing

EQUIPMENTS

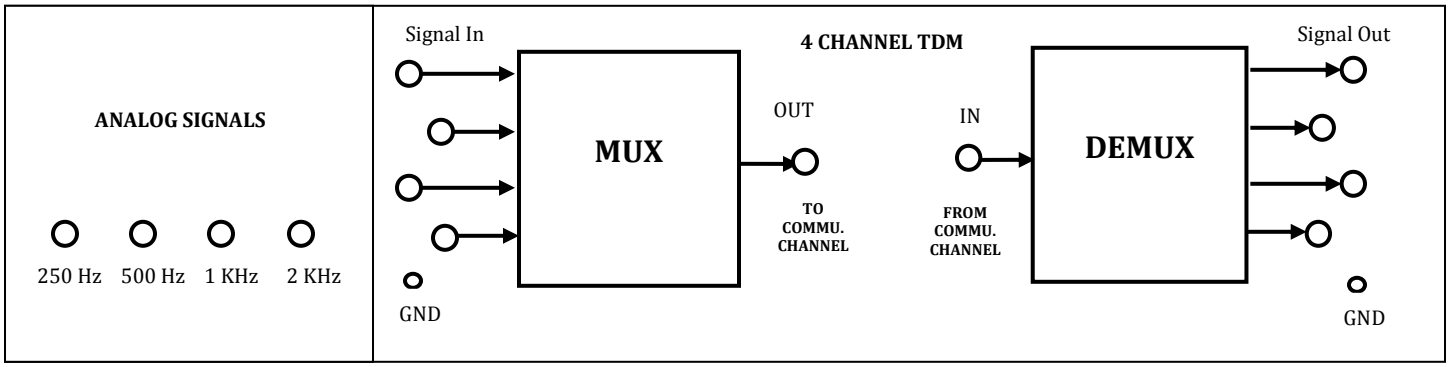
- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

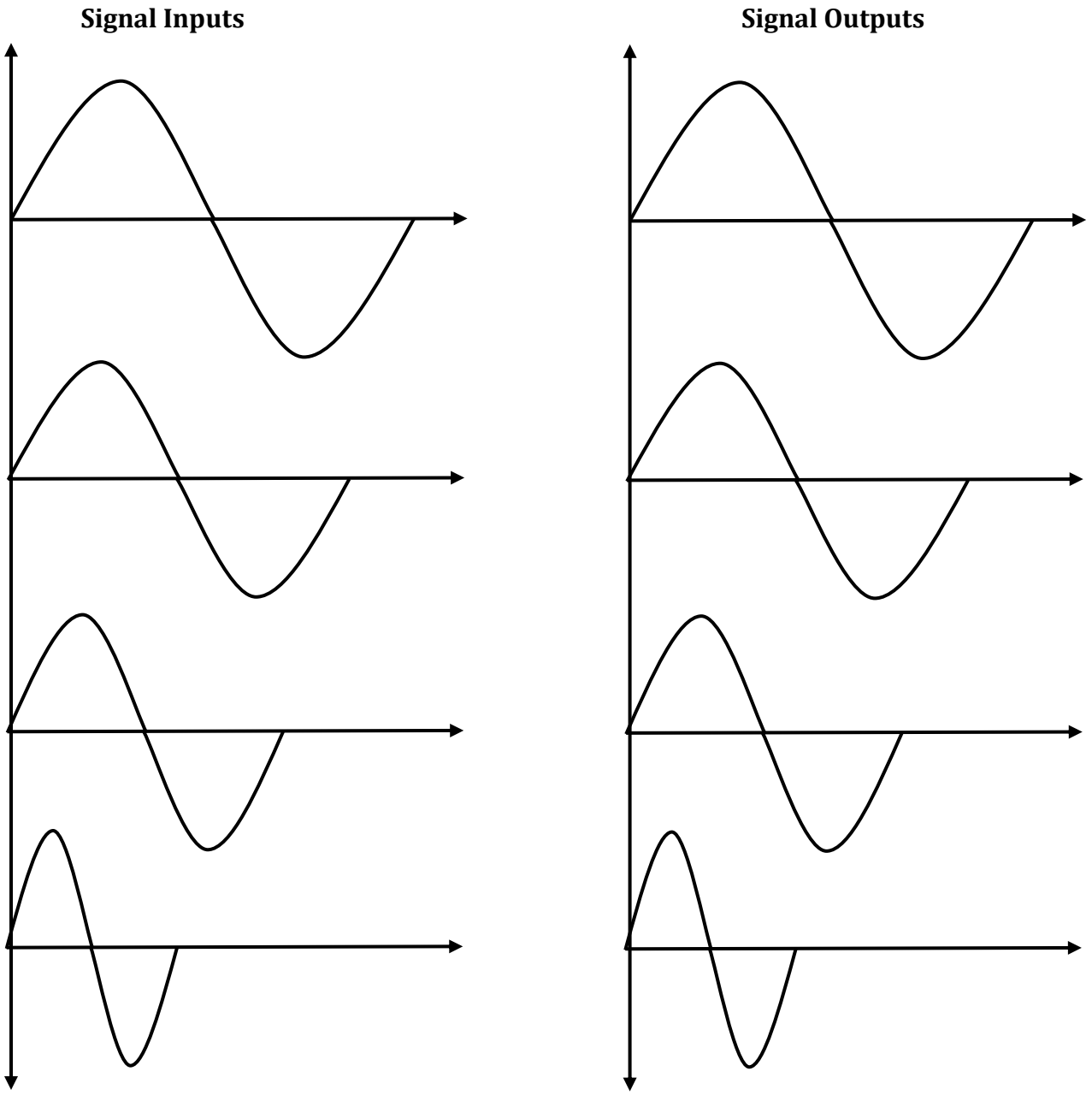
Time-division multiplexing (TDM) is a method of transmitting and receiving independent signals over a common signal path by means of synchronized switches at each end of the transmission line so that each signal appears on the line only a fraction of time in an alternating pattern. It is used when the data rate of the transmission medium exceeds that of signal to be transmitted. This form of signal multiplexing was developed in telecommunications for telegraphy systems in the late 19th century, but found its most common application in digital telephony in the second half of the 20th century.

Time-division multiplexing is used primarily for digital signals, but may be applied in analog multiplexing in which two or more signals or bit streams are transferred appearing simultaneously as sub-channels in one communication channel, but are physically taking turns on the channel. The time domain is divided into several recurrent *time slots* of fixed length, one for each sub-channel. A sample byte or data block of sub-channel 1 is transmitted during time slot 1, sub-channel 2 during time slot 2, etc. One TDM frame consists of one time slot per sub-channel plus a synchronization channel and sometimes error correction channel before the synchronization. After the last sub-channel, error correction, and synchronization, the cycle starts all over again with a new frame, starting with the second sample, byte or data block from sub-channel 1, etc.

BLOCK DIAGRAM



MODEL WAVEFORMS



PROCEDURE

1. Refer to the Block Diagram & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit & switch it on.
3. Connect **250Hz**, **500Hz**, **1 KHz**, and **2 KHz** sine wave signals from the Function Generator to the multiplexer inputs channel by means of the connecting chords provided.
4. Connect the multiplexer output of the transmitter section to the demultiplexer input of the receiver section.
5. Take observations as mentioned.

RESULT

Exp. No.: **Date:**

FREQUENCY SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Frequency shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

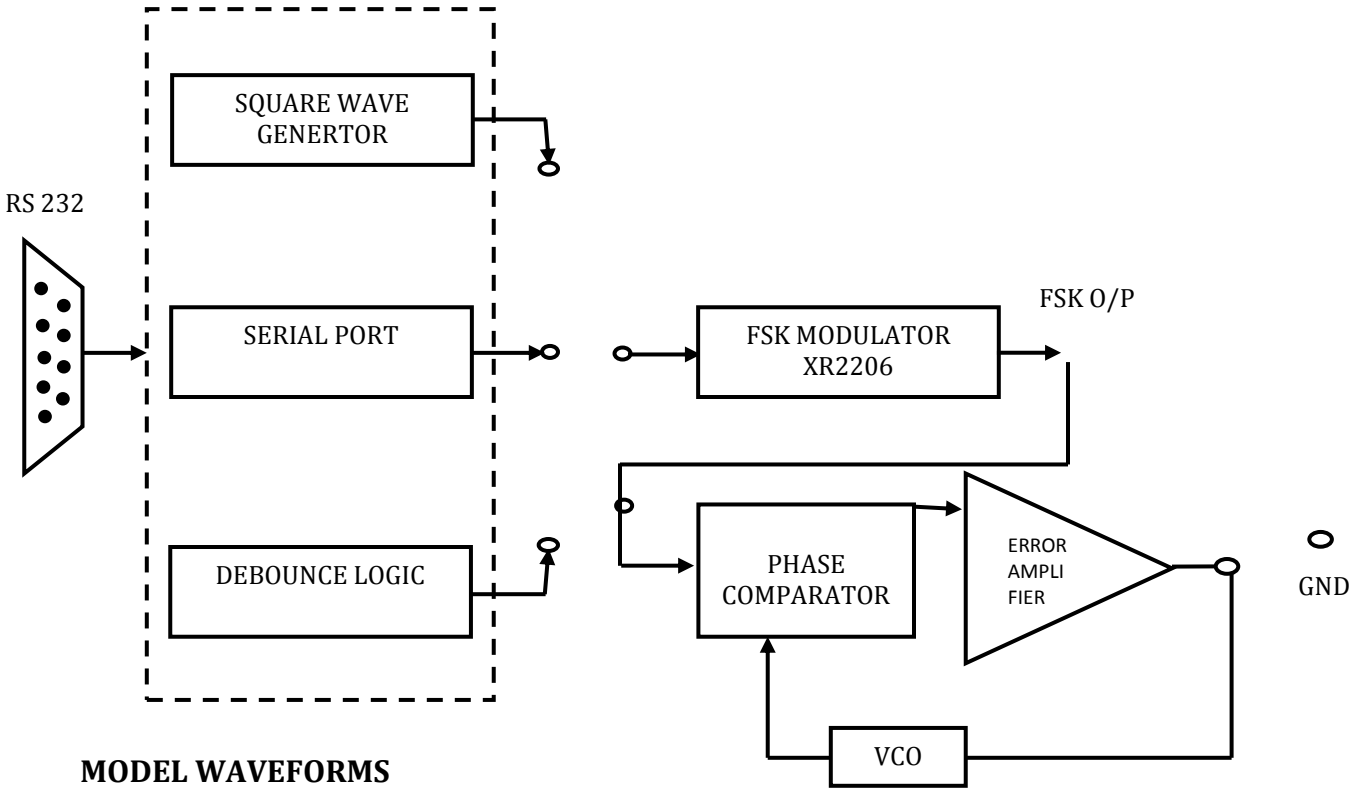
THEORY

Frequency-shift keying (FSK) is the frequency modulation system in which digital information is transmitted through the discrete frequency change of a carrier wave. The technology is used in communication systems such as amateur radio, caller ID, and urgent situation broadcasts. The simplest FSK is binary FSK (BFSK). BFSK uses a pair of discrete frequencies to transmit binary (0s and 1s) information. With this scheme, the "1" is called the mark frequency and the "0" is called the space frequency.

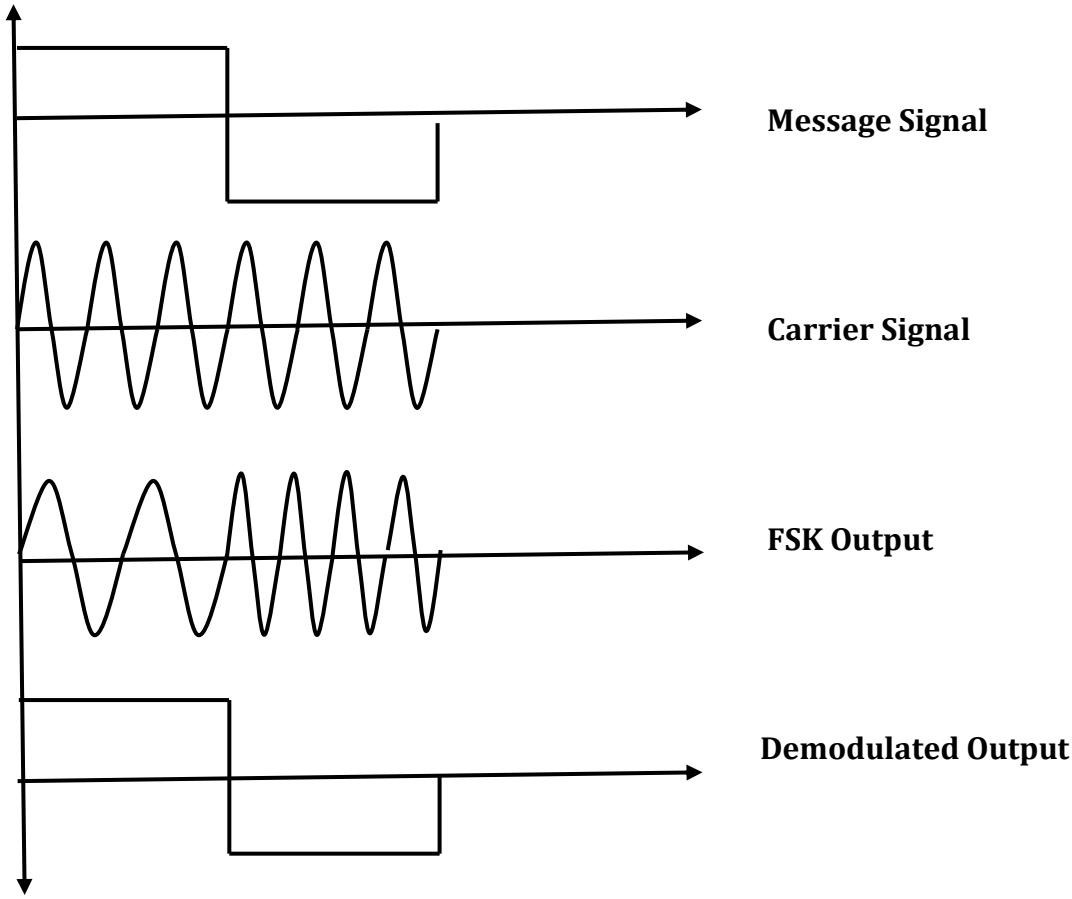
PROCEDURE

1. Switch on experimental kit.
2. Observe the message signal at the output of square wave generator
3. Observe the carrier signal at the output of FSK modulator without applying message.
4. Observe the FSK output at modulator by applying message.
5. Connect the FSK modulated output to the FSK demodulator and observe the output on CRO.

BLOCK DIAGRAM



MODEL WAVEFORMS



RESULT

Exp. No.: **Date:**

PHASE SHIFT KEYING - MODULATION AND DEMODULATION

AIM

To verify Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

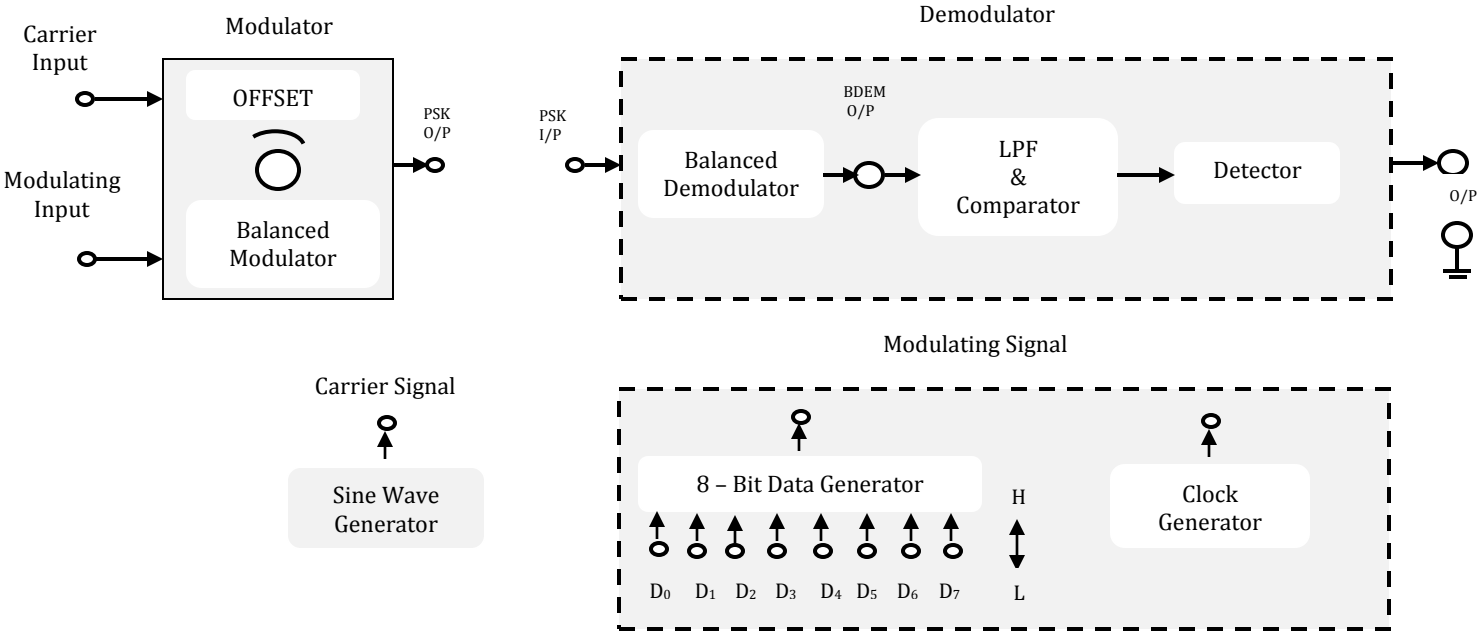
- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

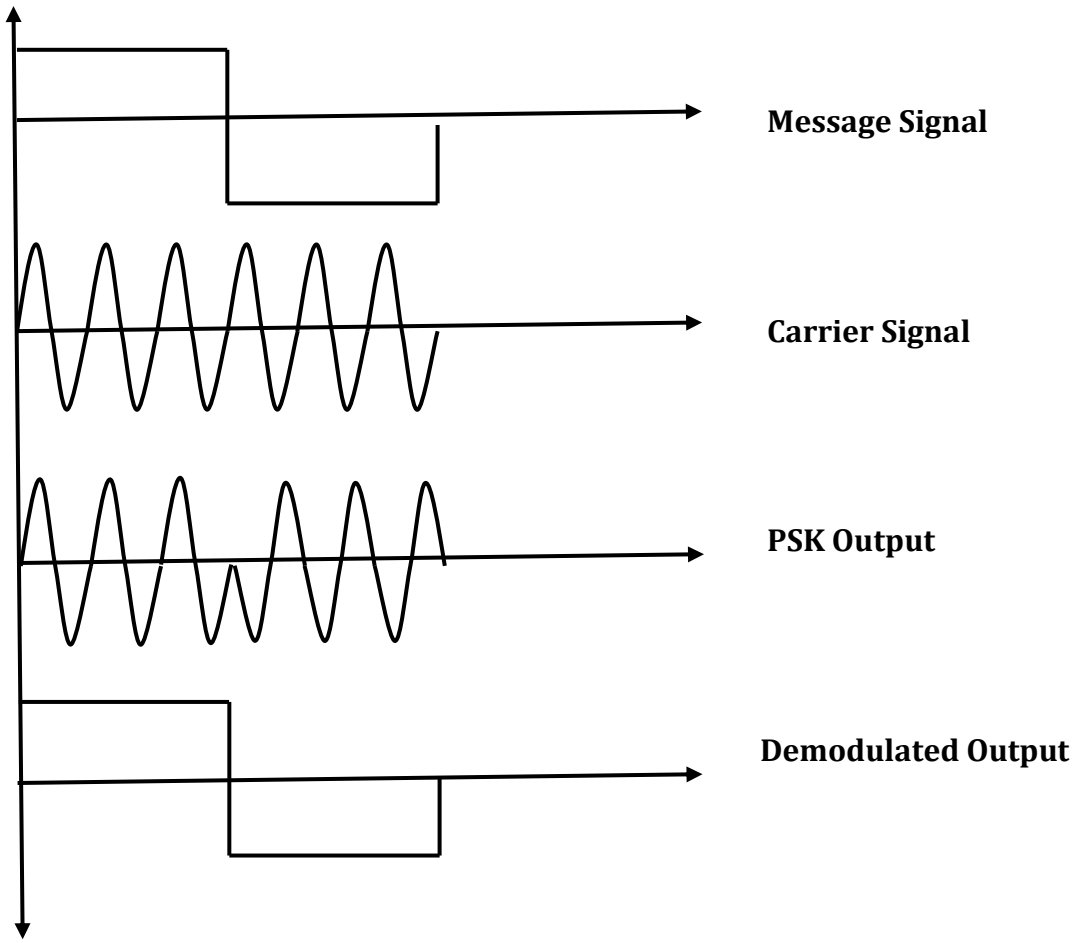
Phase shift keying (PSK) involves the phase shift change of the carrier sine wave between 0º and 180º in accordance with the data stream to be transmitted. PSK is also known as phase reversal keying (PRK).

Functionally, the PSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. Bit in contrast to ASK technique , the digital signal applied to the modulation input for PSK generation is bipolar i.e. have equal positive and negative voltage levels. When the modulating input is positive the output of modulator is a sine wave in phase with the carrier input, Whereas for the negative voltage levels, the output of modulator is a sine wave which is shifted out of phase 180º from the carrier input.

BLOCK DIAGRAM



MODEL WAVEFORMS



PROCEDURE

1. Connect carrier output of carrier generator to carrier input to modulator
2. Connect modulating signal output to modulating input of modulator
3. Switch on experimental kit.
4. Observe the PSK output at modulator and observe PSK output changes accordingly.
5. Connect the PSK modulated output to the PSK demodulator.
6. Connect the output of PSK demodulator to LPF and observe the output on CRO.

RESULT

Exp. No.: **Date:**

DIFFERENTIAL PHASE SHIFT KEYING - MODULATION AND DEMODULATION.

AIM

To verify Differential Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

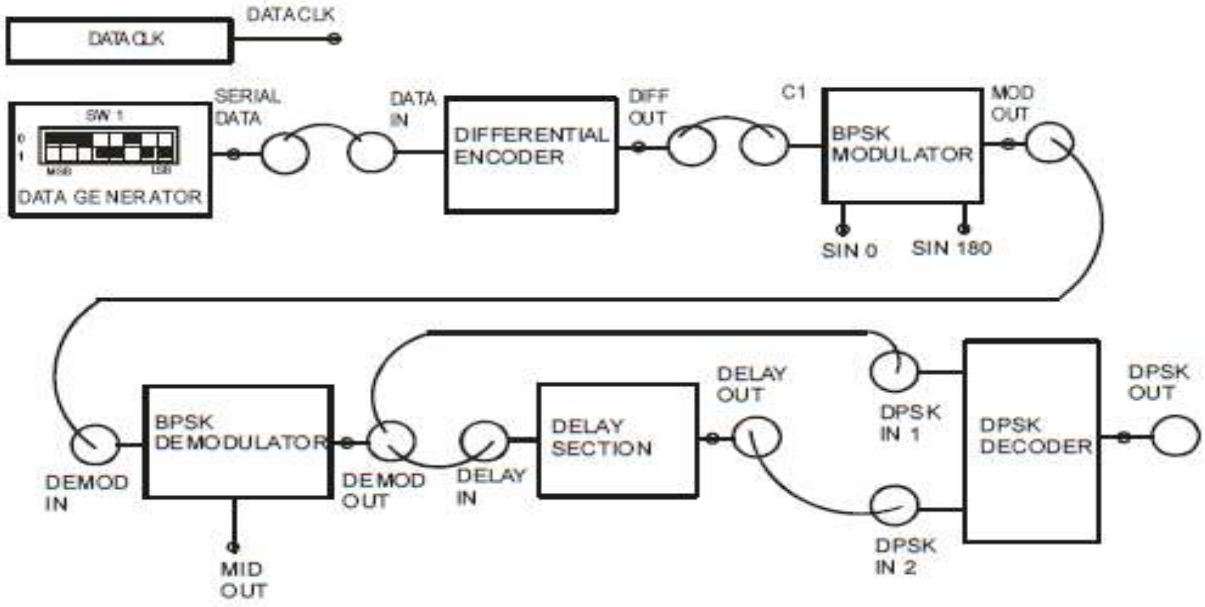
THEORY

In BPSK communication system, the demodulation is made by comparing the instant phase of the BPSK signal to an absolute reference phase locally generated in the receiver. The modulation is called in this case BPSK absolute. The greatest difficulty of these systems lies in the need to keep the phase of the regenerated carrier always constant. This problem is solved with the PSK differential modulation, as the nformation is not contained in the absolute phase of the modulated carrier but in the phase difference between two next modulation intervals.

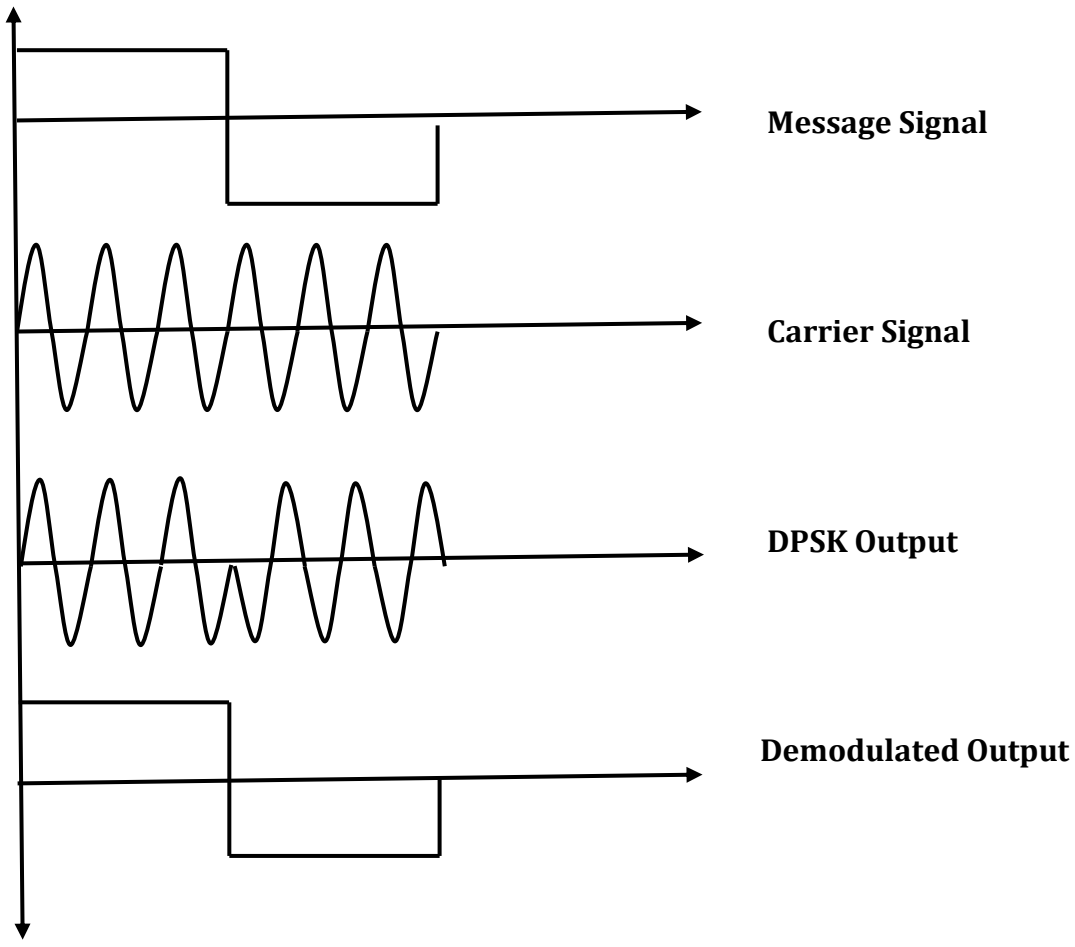
The coding is obtained by comparing the output of an EX-OR, delayed of a bit interval, with the current data bits. As total result of operation, the DPSK signal across the output of the modulator contains 180 deg. phase variation at each data bit "1". The demodulation is made by a normal BPSK demodulator, followed by a DPSK DECODER which is nothing but a decision device supplying a bit "1" each time there is a variation of the logic level across its input.

The DPSK system explained above has a clear advantage over the BPSK system in that the former avoids the need for complicated circuitry used to generate a local carrier at the receiver. To see the relative disadvantage of DPSK in comparison with PSK, consider that during some bit interval the received signal is so contaminated by noise that in a PSK system an error would be made in the determination of whether the transmitted bit was a 1 or 0. in DPSK a bit determination is made on the basis of the signal received in two successive bit intervals. Hence noise in one bit interval may cause errors to two-bit determination. The error rate in DPSK is therefore greater than in PSK, and, as a matter of fact, there is a tendency for bit errors to occur in pairs. It is not inevitable however those errors occur in pairs. Single errors are still possible

BLOCK DIAGRAM



MODEL WAVEFORMS



PROCEDURE

1. Refer to the block diagram and carry out the following connections.
2. Connect power supply in proper polarity to the kit **DCL-DPSK** and switch it on.
3. Select Data pattern of simulated data using switch **SW1**.
4. Connect the **SERIAL DATA** to the **DATA IN** of the **DIFFERENTIAL ENCODER.**
5. Connect differentially encoded data **DIFF OUT** of **DIFFERENTIAL ENCODER** to control input **C1** of **BPSK MODULATOR.**
6. Connect DPSK modulated signal **MOD OUT** of **BPSK MODULATOR** to **DEMOD IN** of the **BPSK DEMODULATOR**.
7. Connect **DEMOD OUT** of **BPSK DEMODULATOR** to **DELAY IN** of **DELAY SECTION** and one input **DPSK IN 1** of **DPSK DECODER**.
8. Connect the **DELAY OUT** of **DELAY SECTION** to the input **DPSK IN 2** of **DPSK DECODER**.
9. Compare the DPSK decoded data at **DPSK OUT** with respect to input **SERIAL DATA.**
10. Observe various waveforms

RESULT

Exp. No.: **Date:**

QUADRATURE PHASE SHIFT KEYING - MODULATION AND DEMODULATION.

AIM

To verify Quadrature Phase shift keying - Modulation and Demodulation.

EQUIPMENTS

- Experimenter kit
- Connecting Chords
- Power supply
- 20 MHz Dual Trace Oscilloscope

THEORY

In this modulation, called Quadrature PSK (QPSK) or 4 PSK the sine carrier takes 4 phase values, separated of 90 deg. and determined by the combinations of bit pair (Dibit) of the binary data signal. The data are coded into Dibit by a circuit generating:

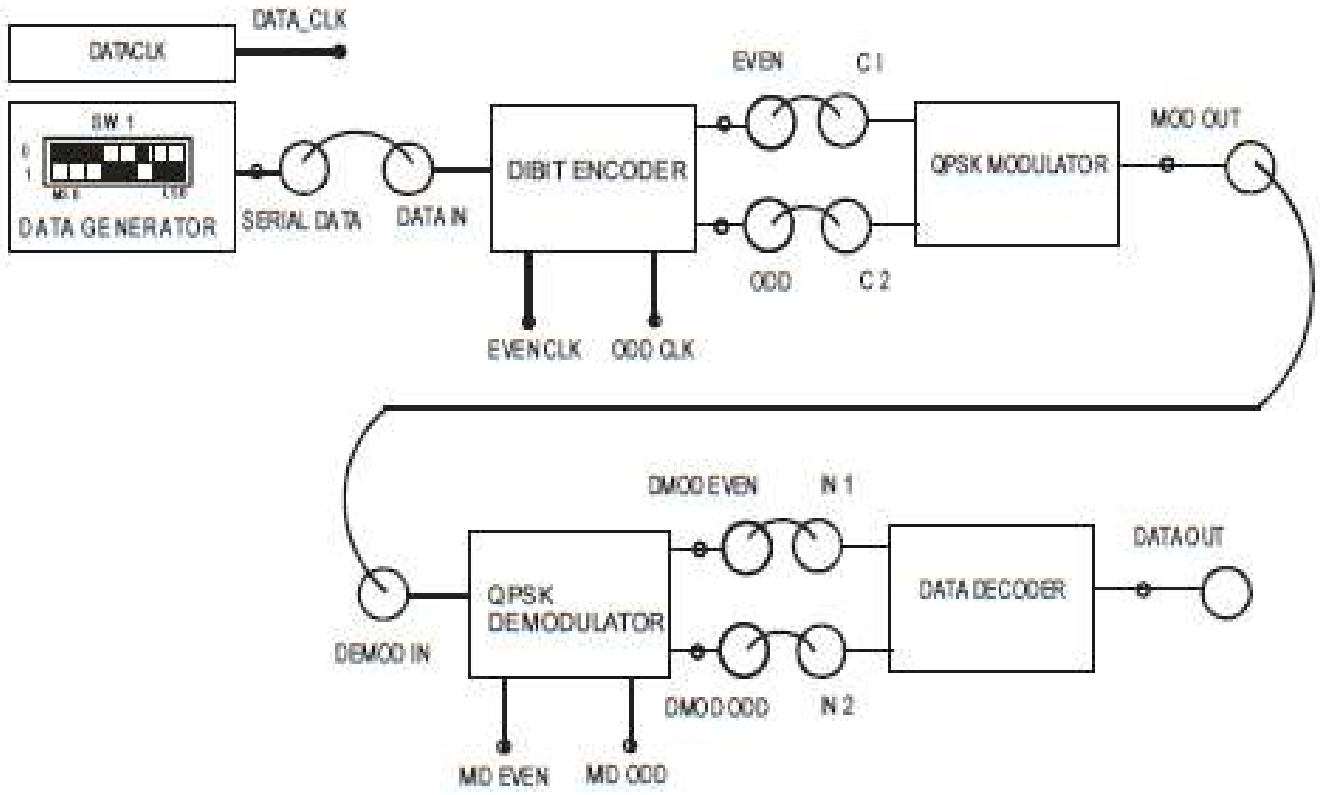
• A data signal **EVEN** (in phase) consisting in voltage levels corresponding to the value of the first bit of the considered pair, for duration equal to 2 bit intervals.

• A data signal **ODD** (in quadrature) consisting in voltage levels corresponding to the value of the second bit of the pair, for duration equal to 2 bit intervals.

The block diagram of the modulator used on the module is shown in the fig. four 1MHz sine carriers, shifted between them of 90 deg, are applied to modulator. The data (signal EVEN & ODD) reach the modulator from the Dibit Encoder. The instantaneous value of EVEN and ODD data bit generates a symbol. Since EVEN and ODD can take either 0 or 1 value, maximum 4 possible symbols can be generated (00, 01, 10, and 11). According to the symbol generated one of the foursine carrier will be selected. The relation between the symbol generated and sine carrier is shown in table.

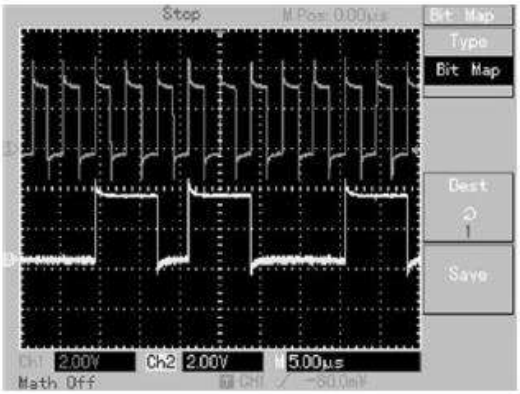
DIBIT		PHASE SHIFT
EVEN	ODD	
0	0	180 deg
0	1	90 deg
1	0	270 deg
1	1	0 deg

BLOCK DIAGRAM



MODEL WAVEFORMS

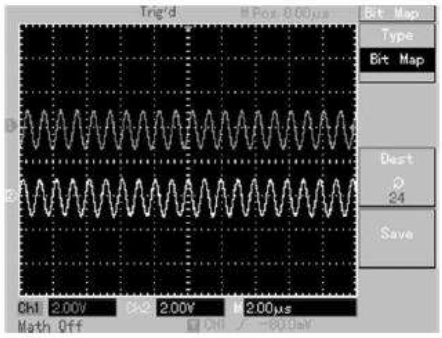
CH 1 : DATA CLK (256 KHz) & CH 2 : SERIAL DATA (00011011)



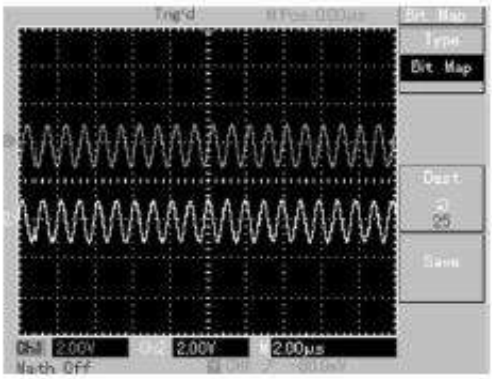
A receiver for the QPSK signal is shown in fig. synchronous detection is required and hence it is necessary to locally regenerate the carriers. The scheme for carrier regeneration is similar to that employed in BPSK. In that earlier case we squared the incoming signal to remove the phase difference, and recovered the data by filtering. The incoming signal is applied to the multipliers to remove the phase shift.

The output of the multipliers can be seen at MID EVEN and MID ODD posts. The output of the multipliers is then given to filters, where we get the recovered even and odd data at the DEMOD EVEN and DEMOD ODD posts. These recovered EVEN & ODD bits having exactly same phase & frequency compared to transmitter EVEN & ODD bit. These EVEN & ODD bits then applied to DATA DECODER logic to recover the original NRZ-L data pattern.

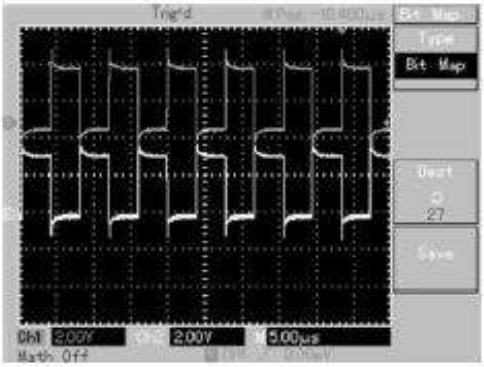
CH 1: SIN 0 (1 MHz) & CH 2: SIN 90 (1 MHz)



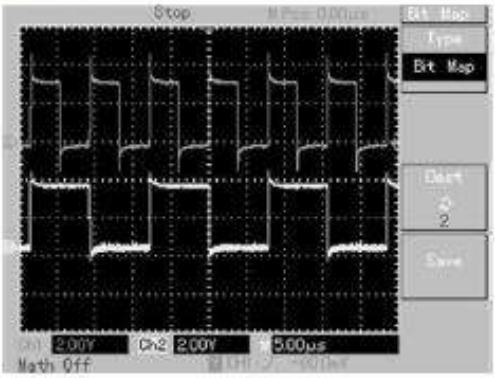
CH 1: SIN 180 (1 MHz) & CH 2: SIN 270 (1 MHz)



CH 1 : EVEN CLK (128 KHz) & CH 2 : ODD CLK (128 KHz)



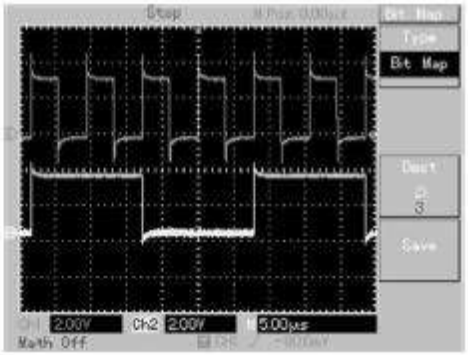
CH 1 : EVEN CLK (128 KHz) & CH 2 : EVEN DATA



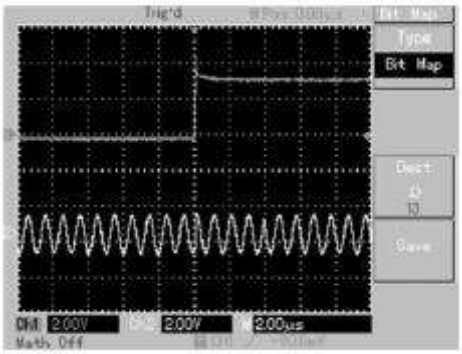
PROCEDURE

1. Refer to the block diagram and carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kits **DCL-QPSK** and switch it on.
3. Select Data pattern of simulated data using switch **SW1**.
4. Connect **SERIAL DATA** generated to **DATA IN** of the **DIBIT ENCODER**.
5. Connect the dibit data **EVEN** & **ODD** bit to control input **C1** and **C2** of **QPSK MODULATOR** respectively
6. Connect QPSK modulated signal **MOD OUT** to the **DEMOD IN** of the **QPSK DEMODULATOR**.
7. Connect **DEMOD EVEN & DEMOD ODD** outputs of **QPSK DEMODULATOR** to **IN 1, & IN 2** posts of **Data Decoder** respectively.
8. Observe various waveforms as mentioned below

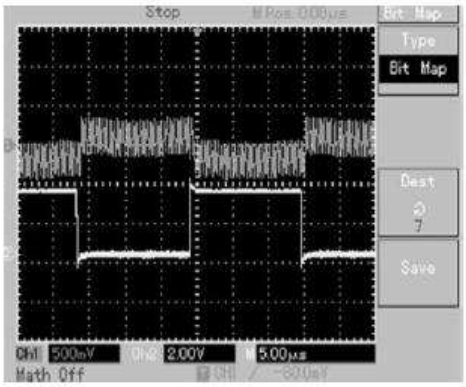
CH 1 : ODD CLK (128 KHz) & CH 2 : ODD DATA



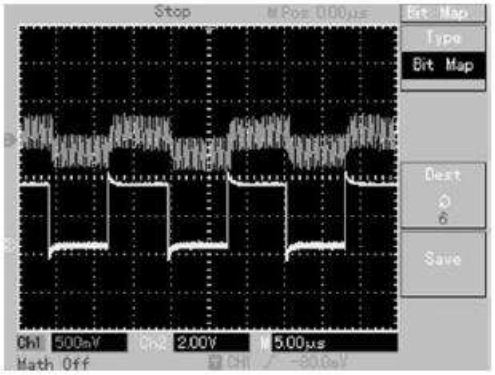
CH 1 : EVEN & CH 2 : MOD OUT



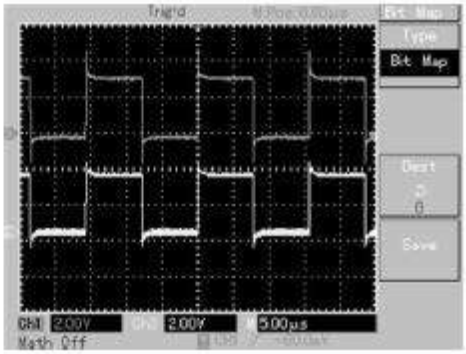
CH 1 : MID ODD & CH 2 : DEMOD ODD



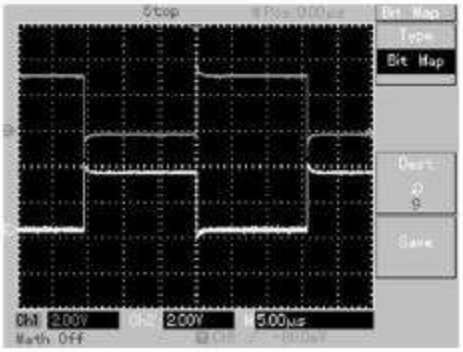
CH 1 :MID EVEN & CH 2 : DEMOD EVEN



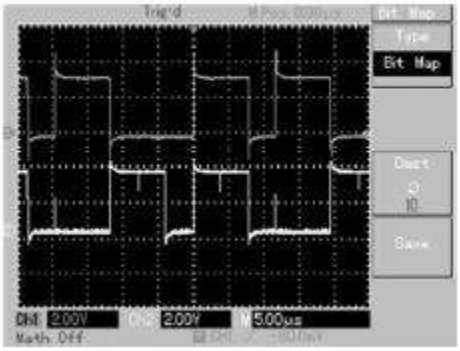
CH 1 : EVEN & CH 2 : DEMOD EVEN



CH 1 :ODD & CH 2 : DEMOD ODD



CH 1 :SERIAL DATA & CH 2 : DATA OUT



RESULT