SRI VENKATESWARA COLLEGE OF ENGINNERING & TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTAPUR)
ACADEMIC REGULATIONS
M.TECH REGULAR 2 YEAR DEGREE PROGRAMME
(FOR THE BATCHES ADMITTED FROM THE ACADEMIC YEAR 2015-16)

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time. Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE/PGECET score, subject to reservations and policies prescribed by the Government from time to time.

2.0 ADMISSION PROCEDURE:

As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows:

a) Category –A seats are to be filled by Convenor through PGECET/GATE score.
b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A.P.

3.0 Specializations:

Sl. No	Department	Specializations
1.	CE	Structural Engg.
2.	EEE	Power Electronics & Electrical Drives
3.	EEE	Electrical Power Systems
4.	ME	CAD/CAM
5.	ME	Machine Design
6.	ECE	VLSI System Design
7.	ECE	Digital Electronics and Communication System
8.	ECE	Embedded systems
9.	CSE	Computer Science &Engg.
10.	CSE	Computer Science
11.	IT	Software Engg.

4.0 COURSE WORK:

4.1. A Candidate after securing admission must pursue the M.Techcourse of study for Four Semesters duration.

4.2. Each semester shall have a minimum of 16 instructional weeks.

4.3. A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

5.0 ATTENDANCE:

5.1. A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance on cumulative basis of all subjects/courses in the semester.

5.2. Condonation of shortage of attendance up to 10% i.e., from 65% and above and less than 75% may be given by the college on the recommendation of the Principal.

5.3. Condonation of shortage of attendance shall be granted only on medical grounds and on representation by the candidate with supporting evidence.

5.4. If the candidate does not satisfy the attendance requirement he is detained for want of attendance and shall reregister for that semester. He shall not be promoted to the next semester.

6.0 EVALUATION:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practical's, on the basis of Internal Evaluation and End Semester Examination.

6.1. For the theory subjects 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation, based on the average of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (first two units) and another immediately after the completion of instruction (last three units) with four questions to be answered out of five in 2 hours, evaluated for 40 marks. For semester end examination (external paper setting & external evaluation) five questions shall be given for a maximum of 60 marks with one question from each unit with internal choice i.e. either or type. All questions carry equal marks.

6.2. For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance (25marks) and practical test at the end of the semester (15marks).

6.3. Seminar is a continuous assessment process. For Seminar there will be an internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts.

6.4. For comprehensive viva voce there will be an internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts.

6.5. A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

6.6. In case the candidate does not secure the minimum academic requirement in any of the subjects (as specified in 6.5) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the subject when next offered or do any other specified subject as may be required.

6.7. **Revaluation / Recounting:**

Students shall be permitted for request for recounting/revaluation of the Semester-End examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised grade sheet. If there are no changes, the same will be intimated to the students.

6.8 **Supplementary Examination:**

In addition to the regular Semester- End examinations conducted, the College may also schedule and conduct supplementary examinations for all the subjects of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

7.0 RE-REGISTRATION:

Following are the conditions to avail the benefit of improvement of internal evaluation marks

7.1. The candidate should have completed the course work and obtained examinations results for I& II semesters.

7.2. He should have passed all the subjects for which the Internal evaluation marks secured are more than or equal to 50%.

7.3. Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

7.4. The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

7.5. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the along with the requisition to the Principal of the college.

7.6. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

8.0 EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ institute.

8.1. Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of I& II Semesters.

8.2. An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor and one internal senior teacher shall monitor the progress of the project work.

8.3. The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4. The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report and award internal assessment marks for 120.

8.5. A candidate shall be allowed to submit the Thesis / Dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva voce examination may be conducted once in two months for all the candidates who have submitted thesis during that period.

8.6. Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor and HOD shall be presented to the H.OD. One copy is to be forwarded to the Controller Of Examinations and one copy to be sent to the examiner.

8.7. The Dept shall submit a panel of three experts for a maximum of 5 students at a time. However, the Thesis / Dissertation will be adjudicated by one examiner nominated by the Chief Controller Of Examinations.

8.8. If the report of the examiner is favorable viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis / dissertation. The board shall jointly award the marks for 180.

8.9. A candidate shall be deemed to have secured the minimum academic requirement in the project work if he secures a minimum of 50% marks in the end viva-voce examination and a minimum aggregate of 50% of the total marks in the end viva-voce examination and the internal project report taken together. If he fails to get the minimum academic requirement he has to appear for the viva-voce examination again to get the minimum marks. If he fails to get the minimum marks at the second viva-voce examination he will not be eligible for

the award of the degree, unless the candidate is asked to revise and resubmit. If the candidate fails to secure minimum marks again, the project shall be summarily rejected.

9.0 Grades, Grade point Average, Cumulative Grade point Average:

9.1. Grade System: After all the components and sub-components of any subject (including laboratory subjects) are evaluated, the final total marks obtained will be converted to letter grades on a "10 point scale" described below.

% of marks obtained	Grade	Grade Points(GP)
90 to 100	A+	10
80 to 89	A	9
70 to 79	B	8
60 to 69	C	7
50 to 59	D	6
Less than 50 in sum of Int. and Ext. (or) Less than 40 in Ext.	F	0
Not Appeared	N	0

9.2. GPA: Grade Point Average (GPA) will be calculated as given below on a "10 Point scale" as an Index of the student's performance at the end of each semester:

$$\textbf{GPA} = \frac{\sum(CXGP)}{\sum C}$$

Where C denotes the credits assigned to the subjects undertaken in that semester and GP denotes the grade points earned by the student in the respective subjects

9.3. CGPA: At the end of every semester, a Cumulative Grade Point Average (CGPA) on a 10 Point scale is computed considering all the subjects passed up to that point as an index of overall Performance up to that Point as given below:

$$\textbf{CGPA} = \frac{\sum(CXGP)}{\sum C}$$

Where C denotes the credits assigned to subjects undertaken upto the end of the current semester and GP denotes the grade points earned by the student in the respective courses.

9.4. Grade sheet: A grade sheet (Marks Memorandum) will be issued to each student Indicating his performance in all subjects registered in that semester indicating the GPA and CGPA. GPA and CGPA will be rounded off to the second place of decimal.

9.5 Transcripts: After successful completion of the entire Program of study, a transcript containing performance of all semesters will be issued as a final record. Duplicate transcripts will also be issued, if required, after payment of requisite fee.

10.0 Award of Degree: The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Anantapur on the recommendation of The Principal of SVCET (Autonomous).

10.1 Eligibility: A student shall be eligible for the award of M.Tech. Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the program of study for which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the specialization of study within the stipulated time.
- Obtained CGPA greater than or equal to 6.0 (Minimum requirement for declaring as passed.)

10.2 Award of Class: Declaration of Class is based on CGPA.

Cumulative Grade Point Average	**Class**
≥7.75	First Class with Distinction
≥6.75 and<7.75	First Class
≥6.0 and <6.75	Second Class

11.0 WITHHOLDING OF RESULTS: If the candidate has not paid dues to the university or

If any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

12.0 TRANSITORY REGULATIONS*:*

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to 6.5 and 4.3 sections. Whereas they continue to be in the academic regulations of the batch they join later.

13.0 GENERAL:

i. The academic regulations should be read as a whole for purpose of any interpretation.

ii. Disciplinary action for Malpractice/improper conduct in examinations is appended.

iii. Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

iv. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

v. The college may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the college.

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Sri Venkateswara College of Engineering And Technology (Autonomous)

R.V.S. Nagar, Chittoor

Identification of Courses

M. Tech

Each course shall be uniquely identified by an alphanumeric code of width 7 characters as given below.

No. of digits	Description
First two digits	Year of regulations Ex:15
Next one letter	Type of program: A: B. Tech B: M. Tech C: M.B.A D: M.C.A
Next two letters	Code of program: ST: Structural Engineering, P.E: Power Electronics & Electric Drives, PS: Electrical Power Systems, CM: CAD/CAM, MD: Machine Design, VL: VLSI, DE: DECS, EM: Embedded Systems, CS: Computer Science and Engineering, CO: Computer Science, SE: Software Engineering,
Last two digits	Indicate serial numbers: ≥ 01

Ex:

15BST01

15BPE01

15BPS01

15BCM01

15BMD01

15BVL01

15BDE01

15BEM01

15BCS01

15BCO01

15BSE01

SRI VENKATESWARA COLLEGE OF ENGINNERING & TECHNOLOGY

(AUTONOMOUS)

(AFFILIATED TO JNTUA, ANANTAPUR)

RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices / Improper conduct	**Punishment**
	If the candidate	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.

3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred and forfeits of seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.

8.	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction or property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.

10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

Sri Venkateswara College of Engineering and Technology (Autonomous)
R.V.S. Nagar, Chittoor-517127.A.P
Course Structure and Syllabi for M.Tech in EMBEDDED SYSTEMS

M.Tech I year I Semester

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BEM01	Microcontrollers Interfacing	3	1	-	4	40	60	100
2	15BCS12	Real Time Operating Systems	3	1	-	4	40	60	100
3	15BEM02	Embedded System Design	3	1	-	4	40	60	100
4	15BDE02	Advanced Digital Signal Processing	3	1	-	4	40	60	100
		Elective-I:							
5	15BVL03	1. Digital IC Design	3	1	-	4	40	60	100
6	15BVL01	2. VLSI Technology							
7	15BEM03	3. System Modeling & Simulation							
		Elective-II:							
8	15BCS19	1. Cloud Computing	3	1	-	4	40	60	100
9	15BVL04	2. Hardware Description Languages							
10	15BCS04	3. Advanced Operating Systems							
11	15BEM04	Microcontrollers Interfacing Lab	-	-	3	2	40	60	100
12	15BEM05	Embedded Systems Lab	-	-	3	2	40	60	100
13	15BEM06	Seminar – I	-	-	-	2	50	-	50
		TOTAL:	**18**	**6**	**6**	**30**	**370**	**480**	**850**

M.Tech I Year II Semester

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BCS10	Cryptography and Network Security	3	1	-	4	40	60	100
2	15BDE01	Digital System Design	3	1	-	4	40	60	100
3	15BVL06	Hardware Software Co-design	3	1	-	4	40	60	100
4	15BDE11	DSP Processors & Architectures	3	1	-	4	40	60	100
		Elective-III:							
5	15BVL12	1. Testing & Testability	3	1	-	4	40	60	100
6	15BEM07	2. Micro Electro Mechanical Systems							
7	15BEM08	3. System on Chip Architectures							
		Elective-IV:							
8	15BVL09	1. FPGA Architectures & Applications	3	1	-	4	40	60	100
9	15BVL13	2. Nano Electronics							
10	15BDE15	3. High Speed Networks							
11	15BEM09	RTOS & FPGA Lab	-	-	3	2	40	60	100
12	15BDE18	Advanced DSP Lab	-	-	3	2	40	60	100
13	15BEM10	Seminar - II	-	-	-	2	50	-	50
14	15BEM11	Comprehensive Viva	-	-	-	2	100	-	100
		TOTAL:	**18**	**6**	**6**	**32**	**470**	**480**	**950**

M.Tech II Year III & IV Semesters

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BEM12	Project Work	-	-	-	12	120	180	300

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

	L	T	P	C
M.Tech- I Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BEM01) MICROCONTROLLERS INTERFACING

Objectives:

1. *To study the distinguish between microprocessors and microcontrollers*
2. *Describe the 68HC11 architecture and programming model*
3. *Identify different types of memory and describe how each is used*
4. *Analyze the assembly code programs*

Outcomes:

After completion of course, the students will be able :

1 *to program a microcontroller to perform various tasks*

2 *to interface a microcontroller to various devices*

3 *to understand microcontroller peripherals*

4 *to design and implement a microcontroller-based embedded system*

UNIT I

INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT II

MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT III

PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I^2C bus, ADC, UART, PIC family parts.

UNIT IV

MICROCONTROLLER INTERFACING:8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller, On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT V

INTERRUPT SYNCHRONIZATION: Interrupt vectors & priority, external interrupt design, Serial I/O Devices,RS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial Communication Controller.

CASE STUDIES: Design of Embedded Systems using the micro controller 8051/ARM6TDMI for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1. M.A. Mazadi& J.G. Mazidi, "The 8051 Micro Controller & Embedded Systems", Pearson Education. Asia (2000).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.

REFERENCES:

1. 8-bit Embedded Controllers, INTEL Corporation 1990.
2. John B.Peatman, "Designing with PIC Microcontrollers", Pearson Education Inc, India, 2005.

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous) **L T P C**
M.Tech- I Semester-Embedded Systems **3 1 0 4**

(15BCS12) REAL TIME OPERATING SYSTEMS

Objectives:

The objective of this course is to make students to:

1. *To cover the principles and design methods of real-time computer systems.*
2. *To covers the interfacing techniques and microprocessor system realization.*
3. *To gain an understanding of how an operating system manages concurrency.*
4. *To develop knowledge of modern operating system practice.*

Outcomes:

At the end of the course the student will be able to:

1. *Students will understand the fundamental elements of thread and process concurrency.*
2. *Students will understand Basic introduction to real-time systems design, development and implementation.*
3. *Students will be able to relate modern industrial-strength operating system design and implementation to general operating system concepts: windows 7,UNIX*

UNIT I

INTRODUCTION TO UNIX: Overview Of Commands, File I/O, (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT II

REAL TIME SYSTEMS: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT III

APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT IV

OPERATING SYSTEMS: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.
RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

UNIT V

FAULT TOLERANCE TECHNIQUES: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time, Integrated Failure Handling.
CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches, Semaphore, Binary Mutex, Counting: Watch Dugs, I/O System.

TEXT BOOKS:

1. Richard Stevens, "Advanced Unix Programming".
2. Jane W.S. Liu, "Real Time Systems", Pearson Education.
3. C.M.Krishna, KANG G. Shin, "Real Time Systems", McGraw.Hill

REFERENCES:

1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
4. http://www.xml.com/ldd/chapter/book.

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

	L	T	P	C
M.Tech- I Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BEM02) EMBEDDED SYSTEM DESIGN

Objectives:

1.To study the overview of embedded system.
2.To know various communication interfacings.
3.To study the scheduling architectures
4.To study the ARM and SHARC processor.

Outcomes:

After the completion of the course,the students will able :

1. *to perform system analysis and architecture design*
2. *to apply embedded concepts on real time applications*
3. *to get knowledge on ARM processor and SHARC processor*
4. *to get an idea about Debugging techniques*

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT III

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT IV

INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankajgupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002.

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	L	T	P	C
M.Tech-I Semester- EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BDE02) ADVANCED DIGITAL SIGNAL PROCESSING

Objectives:

To enable the students

1. *To understand the fast Fourier transform algorithms.*
2. *To understand the design of digital filters.*
3. *To understand the multirate signal processing.*
4. *To understand the finite word length effects in IIR digital filters.*

Outcomes:

The student will

1. *Understand the fundamentals Discrete time Systems.*
2. *Understand the Realization of digital filters.*
3. *Understand the implementation of sampling rate conversion.*
4. *Understand the Applications of Digital Signal Processing.*

UNIT I

OVER VIEW: Discrete-Time Signals, Sequences and sequence Representation, Discrete-Time Systems, Time-Domain Characterization and Classification of LTI Discrete-Time Systems. The Continuous-Time Fourier Transform, The discrete-Time Fourier Transform, energy Density Spectrum of a Discrete-Time Sequence, Band-Limited Discrete-Time signals, The Frequency Response of LTI Discrete-Time System.

DSP ALGORITHEMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform

UNIT II

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

DIGITAL FILTER SRTUCTURE AND DESIGN: All Pass Filters, Tunable IIR Digital Filter, IIR Tapped Cascade Lattice Structures, FIR Cascaded Lattice Structures, Parallel All Pass Realization of IIR Transfer Functions, State Space Structures, Poly phase Structures, Digital Sine-Cosine Generator, Computational Complexity of Digital Filter Structures, Design of IIR Filter using pade' approximation, Least Square Design Methods, Design of Computationally Efficient FIR Filters.

UNIT III

MULTIRATESIGNALPROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

ANALYSIS OF FINITE WORD LENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arithmetic–ADC quantization noise & signal quality-Finite word length effect in IIR digital Filters–Finite word-length effects in FFT algorithms.

UNIT IV

POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between autocorrelation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT V

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Non stationary Signals, Musial Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete-Time Analytic Signal Generation.

TEXTBOOKS:

1. Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications.
2. Digital Signal Processing Principles, Algorithms, Applications by J G Proakis, D G Manolokis, PHI.

REFERENCES:

1. Discrete-Time Signal Processing by A V Oppenhiem, R W Schafer, Pearson Education.
2. DSP- A Practical Approach- Emmanuel C Ifeacher Barrie. W. Jervis, Pearson Education.
3. Modern spectral Estimation techniques by S.M.Kay,PHI,1997.

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(Autonomous) **L T P C**
M.Tech- I Semester- EMBEDDED SYSTEM **3 1 0 4**
(15BVL03) DIGITAL IC DESIGN
(Elective – I)

Objectives:

1. To analyze static and dynamic characteristics of CMOS inverter.
2. To understand the sizing of transistors to optimize performance or power.
3. To analyze and design of SRAM and DRAM.
4. To design sub system components.

Outcomes:

After completion of the course, the student will be able to:
1. Analyze the static and dynamic characteristics of CMOS inverter.
2. Solve problems in the design of CMOS logic circuits, with reference to speed and power Consumption.
3. Analyze the static and dynamic characteristics of BICMOS circuits.
4. Design the fundamental blocks of VLSI circuits, both by circuit schematic and physical layout.

UNIT I
CMOS inverters - Static and dynamic characteristics, Static and Dynamic CMOS design, Domino and NORA logic - Combinational and sequential circuits.

UNIT II
Method of Logical Effort for transistor sizing, power consumption in CMOS gates. Arithmetic circuits in CMOS VLSI - Adders- multipliers - shifter.

UNIT III
CMOS memory design - SRAM and DRAM. Bipolar gate Design - BiCMOS logic - static and dynamic behavior - Delay and power consumption in BiCMOS Logic.

UNIT IV
LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V
SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:
1. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 1997
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design",MGH, Second Ed., 1999
3. Douglas A. Pucknell and Kamran Eshraghian "Basic VLSI Design", PHI, 2013.

REFERENCES:
1.Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000
2. Neil H E West and Kamran Eshranghian," Principles of CMOS VLSI Design: A System Perspective", Addision-Wesley 2nd Edition,2002.
3.R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.

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M.Tech -I Semester-EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BVL01) VLSI TECHNOLOGY
(Elective – I)

Objectives:

1. *To introduce basic NMOS, CMOS & Bi-CMOS logic.*
2. *To study electrical properties of MOS devices.*
3. *To understand the design of Low power gates*.
4. *To analyze the combinational and sequential* system design

Outcomes:

After completion of the course, the student will
1. *Gain knowledge of different VLSI fabrication processes and CMOS Logic Design.*
2. *be able to Design different MOS logical circuits.*
3. *be able to know the various tools in the layout analysis*
4. *be able to know about Floor planning methods.*

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: Technology (MOS, CMOS, Bi-CMOS) Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds Relationships, Threshold Voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT IV

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNITV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghianet .al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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M.Tech -I Semester-EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BEM03) SYSTEM MODELING & SIMULATION
(ELECTIVE I)

Objectives:

1. *To introduce basic Simulation Modeling Systems, Models and Simulation.*
2. *To introduce modeling time driven systems.*
3. *To understand markov process.*
4. *To analyze various event driven models.*

Outcomes:

After completion of the course, the student will

1. *will be able to know about basic Simulation Modeling Systems, Models and Simulation.*
2. *be able to Design modeling time driven systems.*
3. *be able to understand markov process.*
4. *be able to analyze various event driven models.*

UNIT I
INTRODUCTION

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT II

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT III

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

MARKOV PROCESS: Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT IV

EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT V

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. System Modeling & Simulation, an Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCES:

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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	L	T	P	C
M.Tech -I Semester-EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BCS19) CLOUD COMPUTING
(ELECTIVE II)

Objectives:

The Objective of this course is to make students to

1. *Learn fundamental ideas behind Cloud Computing, the evolution of the paradigm, its applicability; benefits, as well as current and future challenges;*
2. *Learn about cloud storage technologies and relevant distributed file systems;*
3. *Understand the emerging area of "cloud computing" and how it relates to traditional models of computing.*
4. *Gain competence in Map Reduce as a programming model for distributed processing of large datasets*.

Outcomes:

At the end of course student should be able to

1. *Articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art cloud computing*
2. *Identify the architecture and infrastructure of cloud computing, including SaaS, PaaS, IaaS, public cloud, private cloud, hybrid cloud, etc.*
3. *Explain the core issues of cloud computing such as security, privacy, and interoperability.*
4. *Choose the appropriate technologies, algorithms, and approaches for the related issues.*

UNIT I
Overview of Cloud Computing: Meaning of the terms cloud and cloud computing, cloud based service offerings, Grid computing vs Cloud computing, Benefits of cloud model, limitations, legal issues, Key characteristics of cloud computing, Challenges for the cloud, The evolution of cloud computing.

UNIT II
Web services delivered from the cloud: Infrastructure as a service, Platform-as-a-service, Software-as-a-service. Building Cloud networks: Evolution from the MSP model to cloud computing and software -as-a-service, The cloud data center, SOA as step toward cloud computing, Basic approach to a data center based SOA.

UNIT III
Federation Presence, Identity and Privacy in the cloud: Federation in the cloud, Presence in the cloud, Privacy and its relation to cloud based information system. Security in the Cloud: Cloud security challenges, Software-as-a-service security. Common Standards in Cloud computing: The open cloud consortium, The distributed management task force, standards for application developers, standards for messaging, standards for security.

UNIT IV
End user access to cloud computing: youtube, zimbra, Facebook, Zoho, DimDim Collaboration Mobile internet devices and the cloud: Smartphone, mobile operating systems for smart phones, Mobile Platform virtualization, Collaboration applications for mobile platforms, Future trends.

UNIT V
Virtualization: Adding guest Operating system. Cloud computing, Downloading open Solaris as a Guest OS, Using the 7-Zip Archive Tool casestudies1: Amazon EC2, Amazon simple DB,: Google App Engine.

TEXT BOOKS:

1. John W. Rittinghouse, James F. Ransome ,"*Cloud Computing implementation, management and security*", CRC Press, Taylor &Francis group, 2010.
2. Anthony T.velte, TobJ.velte Robert Elsenpeter, "*Cloud Computing: A practical approach*", Tata McGraw Hill edition, 2010.

REFERENCES:

1. George Reese, *Cloud Application Architectures Building Applications and Infrastructure in the Cloud*, O'Reilly Media Released, April 2009.
2. David S. Linthicum ,"*Cloud Computing and SOA convergence in your enterprise*", Addison-Wesley.

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M.Tech- I Semester- EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BVL04) HARDWARE DESCRIPTION LANGUAGES
(ELECTIVE – II)

Objectives:

1. *To understand various modeling in HDL.*
2. *To design digital circuits using Verilog HDL.*
3. *To understand Verilog data types , operators in Verilog HDL.*
4. *To understand synthesis in Verilog HDL.*

Outcomes:

After completion of the course, the student will be able to:

1. *Analyze the various design methodologies in HDL.*
2. *Program in Verilog HDL for digital circuits.*
3. *Analyze the synthesis of digital circuits.*
4. *Design the digital circuits in Verilog HDL.*

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives – Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT V

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

TEXT BOOKS:

1. M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.NAWABI, "VHDL Analysis and Modeling of Digital Systems", (2/E), McGraw Hill, 1998.

REFERENCES:

1. M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. PERRY, "VHDL", (3/E), McGraw Hill.

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	L	T	P	C
M.Tech- I Semester- EMBEDDEDSYSTEMS	**3**	**1**	**0**	**4**

(15BCS04) ADVANCED OPERATING SYSTEMS
(ELECTIVE – II)

Objectives:

The objective of this course is to make students to:

1. *To develop an understanding of basic operating system concepts.*
2. *To gain an understanding of how an operating system manages concurrency.*
3. *To develop a knowledge of modern operating system practice*

Outcomes:

At the end of the course the student will be able to:

1. *Students will Understand basic operating system concepts: computer and operating system structures, process Management, storage Management, protection.*
2. *Students will understand the fundamental elements of thread and process concurrency.*
3. *Students will be able to relate modern industrial-strength operating system design and implementation to general operating system concepts: windows 7,UNIX*

UNIT I

INTRODUCTION: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware

UNIT II

PROCESS SCHEDULING: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock-occurrence, prevention, detection and recovery;

UNIT III

STORAGE MANAGEMENT: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

FILE SYSTEM MANAGEMENT: File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery;

UNIT IV

I/O MANAGEMENT: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP;

UNIT V

OS SECURITY: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

CASE STUDIES: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX; Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

TEXT BOOKS:

1. DietalH.M , "An Introduction to OS" Pearson Education pvt.Ltd/PHI New Delhi, 12th Indian Reprint 2003.
2. Andrew S.Tanenbaum, "Modern OS"PHI Pearson Education pvt.Ltd New Delhi, 3rd Indian Reprint 2004.
3. Silberschatz . A, Galvin.p and Gagne.G, "Operating System Concepts", John Wiley and Sons. Singapore,2002.

REFERENCES:

1. William Stallings, "Operating Systems", Pearson Education pvt.Ltd.
2. D.M. Dhamdhere,"Operating Systems – A Concept Approach", Tata McGraw Hill, 2003.

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	L	T	P	C
M.Tech - I Semester-EMBEDDED SYSTEMS	**0**	**0**	**3**	**2**

(15BEM04) MICROCONTROLLERS INTERFACING LAB

Objectives:

1. *To provide students with the concepts and techniques required in designing computer hardware interfaces and embedded software for microcontrollers.*
2. *to design and implement a microcontroller-based embedded system*
3. *to provide practical hands-on experience with microcontroller's applications and interfacing techniques*

Outcomes:

After completion of this course the student will be able to:

1. Use assembly languages in developing programs for the use of microcontrollers.
2. Understand the fundamentals of microcontroller systems and interface, and have the ability to apply them.
3. Identify, formulate and solve problems by using the concepts of microcontroller systems and interface.

Note: Minimum 12 experiments are to be conducted

1. An 8051 Alp to Clear a Register and Add 3 to it Ten Times and Store the Result in memory.
2. Find the Largest Number in an array.
3. Arrange the array of numbers in ascending order.
4. To convert 8 bit two digit BCD number system into Hexadecimal number system.
5. HEX to ASCII conversion.
6. To convert the given hexadecimal value to its equivalent BCD conversion.
7. To interface the LCD display with 89C51 microcontroller and to verify data on LCD display.
8. To interface two seven segment LED display in 89C51 microcontroller and to verify data on LED display.
9. To transfer the data serially between two microcontroller kit using RS232C.
10. To interface the stepper motor with 89C51 microcontroller and to rotate it in clockwise direction.
11. Write a program to use the Port pins P1.0 and P1.1 as input, P1.4, P1.5, P1.6 and P1.7 are output.
12. Write a program to use the **TIMER 0** as a counter
13. Write a program using EX0 interrupt function.
14. To interface the 4 x 4 matrix keyboard with the 89C51 microcontroller and to verify the output.

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(Autonomous)

	L	T	P	C
M.Tech- I Semester-EMBEDDED SYSTEMS	**0**	**0**	**3**	**2**

(15BEM05) EMBEDDED SYSTEMS LAB

Objectives:

1. *To introduce the students to program the 8051 and their interfaces*
2. *To analyze programs and various devices using KIEL*
3. *To provide a platform for the students to do multidisciplinary projects*

Outcomes:

After completion of the course, the students will able:

1. *To perform interfacing using LED &LCD.*
2. *To perform the program using assembly & C Languages.*
3. *To perform serial transmission& Reception.*

ASSEMBLY:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7. Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.

3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.

4. LED'S
   (A) Blinking led
   (B) Dancing led's

5. LCD interface

6. Serial Communication
   A) Serial Transmission
   B) Serial Reception

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M.Tech- I Semester-EMBEDDED SYSTEMS	**0**	**0**	**0**	**2**

(15BEM06) SEMINAR- I

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

M.Tech- II Semester –EMBEDDED SYSTEM

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(15BCS10) - CRYPTOGRAPHY AND NETWORK SECURITY

Objectives:

1. *To understand the importance and application of each of confidentiality, Integrity,*
2. *authentication and availability*
3. *To understand various cryptographic algorithms.*
4. *To understand the basic categories of threats to computers and networks*

Outcomes:

At the end of the course the student will be able to:

1. *Various cryptographic standards and algorithms.*
2. *Designing the security system for small scale business applications*
3. *Designing authorization systems for verification purpose*
4. *Design firewalls and trusted systems.*

UNIT I

Security Goals, Security Attacks (Interruption, Interception, Modification and Fabrication), Security Services (Confidentiality, Authentication, Integrity, Non-repudiation, Access Control and Availability) and Mechanisms, A model for Internetwork security, Internet Standards and RFCs, Mathematical Tools for Cryptography: Introduction to number theory, Prime & relative numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Chinese remainder theorem, Discrete logarithms.

UNIT II

Conventional Encryption Principles & Algorithms (DES, AES, RC4), Block Cipher Modes of Operation, Location of Encryption Devices, Key Distribution, Public key cryptography principles, Public key cryptography algorithms (RSA, RABIN, ELGAMAL, Diffie-Hellman, ECC), Key Distribution.

UNIT III

Approaches of Message Authentication, Secure Hash Functions (SHA-512, WHIRLPOOL) and HMAC - Digital Signatures: Comparison, Process- Need for Keys, Signing the Digest, Services, Attacks on Digital Signatures, Kerberos, X.509 Directory Authentication Service.

UNIT IV

Network Management, Basic concepts of SNMP, SNMPv1 Community facility and SNMPv3 OS Security, OS Security Functions, Separation, Memory Protection, Access Control, Trusted Operating System: MAC, DAC, Trusted path, Trusted Computing Base.

UNIT V

Viruses and related threats, Anatomy of Virus, Virus Counter Measures - Software Flaws: Buffer Overflow, Incomplete Mediation, Race Conditions, Malware: Brain, Morris Worm, Code Red, Malware Detection - Firewalls, Design principles, Types of Firewalls, Firewall Architectures, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "*Network Security Essentials (Applications and Standards),* Pearson Education.
2. Mark Stamp "*Information Security Principles & Practice*, WILEY INDIA 2006.

REFERENCE BOOKS:

1. Stallings, Cryptography and network Security, Fourth edition, PHI/Pearson
2. Behrouz A. Forouzan" Cryptography& Network Security, TMH 2007.

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M.Tech - II Semester-EMBEDDED SYSTEM

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(15BDE01) DIGITAL SYSTEM DESIGN

Objectives:

Students are able to

1. Know different Hardware description languages.
2. Understand fault classes and fault models of the digital circuits.
3. Know test pattern generation techniques and algorithms.
4. Understand optimization techniques in Programmable logic arrays

Outcomes:

After completion of the course, the students will

1. able to design digital circuit using different levels of modeling in HDL.
2. able to fault model digital circuits
3. familiarize different commercially available PLDs.
4. able to design optimized programmable logic arrays

UNIT I

DESIGNOFDIGITALSYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIALCIRCUITDESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT II

FAULTMODELING: Fault classes and models–Stuck at faults, bridging faults, transition and intermittent faults.

TESTGENERATION: Fault diagnosis of Combinational circuits by conventional methods–Path Sensitization technique, Boolean difference method, Kohavi algorithm.

TESTPATTERNGENERATION: D–algorithm, PODEM, Random testing, transition count testing, Signature Analysis and testing for bridging faults.

UNIT III

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT IV

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

PLATESTING: Fault models, Test generation and Testable PLA design.

UNIT V

ASYNCHRONOUS SEQUENTIALMACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:

1. Z. Kohavi –"Switching & finite Automata Theory"(TMH)
2. N.N.Biswas–"Logic Design Theory"(PHI)
3. Nolman Balabanian, Bradley Calson–"Digital Logic Design Principles"–Wily Student Edition2004.

REFRENCES:

1. M. Abramovici, M.A.Breues,A.D.Friedman–"Digital System Testing and Testable Design", Jaico Publications
2. Charles H. RothJr.–"Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson–"Computer Aided Logic Design"–Wiley4thEdition.

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	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BVL06) HARDWARE SOFTWARE CO- DESIGN

Objectives:

1. *To introduce the hardware/software codesign to the practicing design*
2. *Provides key codesign concepts and attempts to show the benefits of the codesign approach over the current design process.*
3. *Fundamentals, the Design Space of Custom Architectures, the Hardware/software Interface and Application Examples.*
4. *Techniques are used to partition a system into hardware and software components*

Outcomes:

After completion of course, the students will be able to

1. *Design environment that helps the reader to perform experiments in hardware/software codesign.*
2. *partition a system into hardware and software components by using techniques*
3. *to understand various system level specifications*
4. *understand design Issues, Trends, and Considerations*

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware- software partitioning, Distributed system co-synthesis.

UNIT II

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, Prototyping and emulation environments, Future developments in emulation and prototyping.

TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR

ARCHITECTURES: Modern Embedded architectures, Embedded software development needs, Compilation technologies, Practical consideration in a compiler development environment.

UNIT IV

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, The co-design computational model, Concurrency coordinating concurrent computations, Interfacing components, Design verification, Implementation verification, Verification tools and interface verification

UNIT V

LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – level specification, Design representation for system level synthesis, System level specification languages,

LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation, The cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers.

REFERENCE BOOK:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
2. Giovanni, Wayne Wolf, "Readings in Hardware Software Co – design", Academic Press, 2002.

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	L	T	P	C
M.Tech-II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BDE11) - DSP PROCESSORS AND ARCHITECTURES

Objectives:

1. To introduce the basic concepts of DSP
2. To introduce the concepts of DSP Processor and its architectures.
3. To implement the basic DSP algorithms using DSP processor
4. To understand Interfacing memory and I/O devices to programmable DSP devices.

Outcomes:

At the end of this course, the students will be able to understand about the

1. DSP Processors- TMS320C544XX.
2. Implementation of basic DSP algorithms using DSP Processors.
3. Various bus architectures and memory
4. Memory interfacing to Programmable DSP devices

UNIT-I

Introduction to Digital Signal Processing: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX Processors, Memory space, Program Control, Instructions and Programming, On-Chip Peripherals, Interrupts and Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Implementations of Basic DSP Algorithms: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, A COURSE CODEC interface circuit, COURSE CODEC programming, A COURSE CODEC-DSP interface example.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, *Digital Signal Processing*, Thomson Publications, 2004.
2. Lapsley et al, *DSP Processor Fundamentals, Architectures & Features,* S. Chand & Co, 2000.

REFERENCES:

1. Jonathan Stein, *Digital Signal Processing*, John Wiley, 2005.
2. B. VenkataRamani and M. Bhaskar, *Digital Signal Processors, Architecture, Programming and Applications*, TMH, 2004.

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	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BVL12) - TESTING & TESTABILITY
(ELECTIVE – III)

Objectives:

1. To introduce the different modeling styles in digital circuits.
2. To understand the fundamentals of fault detection in digital circuits.
3. To know the basic principles of test vector generation.
4. To understand the principle of boundary scan standards.

Outcomes:

After completion of the course, the student will be able to:

1. Describe the levels of modeling in digital circuits.
2. Get knowledge on single stuck faults and multiple stuck faults.
3. Understand the different testing architectures.
4. Identify faulty components with in a circuit.

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs in Combinational and Sequential Circuits, Functional Testing With Specific Fault Models

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board Level and System Level DFT Approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO, Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test Requirements for MBIST.

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1.Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.

REFERENCES:

1.RobertJ.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.
2.Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.
3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BEM07) MICRO ELECTRO MECHANICAL SYSTEMS
(ELECTIVE III)

Objectives:

1. *To introduce the concepts of micro electromechanical devices.*
2. *To know the fabrication process of Microsystems.*
3. *To know the design concepts of micro sensors and micro actuators.*
4.
5. *To introduce concepts of quantum mechanics and nano systems.*

Outcomes:

After completion of the course ,the student will be able

1. *To know the concepts of MEMS device.*
2. *To know the fabrication process of Microsystems.*
3. *To know the design concepts of micro sensors and micro actuators.*
4. *To know the concepts of quantum mechanics and nano systems.*

UNIT I
OVERVIEW AND INTRODUCTION

New trends in Engineering and Science: Micro and Nano scale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Micro electromechanical Systems, Applications of Micro and Nano electromechanical systems, Micro electromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals

UNIT II
MEMS FABRICATION TECHNOLOGIES

Micro system fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III
MICRO SENSORS

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Micro sensors, Case study: Piezo-resistive pressure sensor

UNIT IV
MICRO ACTUATORS

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators

UNIT V
NANOSYSTEMS AND QUANTUM MECHANICS

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wave unction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits

TEXT BOOKS:

1. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997.
2. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001

REFERENCES:

1. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.
2. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006,
3. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002

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	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BEM08) SYSTEM ON CHIP ARCHITECTURES
(ELECTIVE III)

Objectives:

1. *To understand the fundamental concepts of processor and architecture.*
2. *To learn the AES algorithm design and evaluation.*
3. *To understand the SoC memories and types of utilization.*
4. *To study about SoC buses,reconfiguration technologies.*

Outcomes:

After completion of course, the students will be able :

1. *to know about SoC design architecture and complexity.*
2. *to have an idea on organization of different memories and utilization.*
3. *to get knowledge on re-configuration technologies and mapping designs.*
4. *to apply AES algorithms in applicable areas.*

UNIT I

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing, System level interconnection, An approach for SoC Design, System Architecture and Complexity.

UNIT II

Processors:

Introduction , Processor Selection for SoC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SoC:

Overview of SoC external memory, Internal Memory, Size, Scratch pads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SoC Memory System, Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SoC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SoC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V

Application Studies / Case Studies:

SoC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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	L	T	P	C
M.Tech- II Semester- EMBEDDED SYSTEM	**3**	**1**	**0**	**4**

(15BVL09) FPGA ARCHITECTURES & APPLICATIONS
(ELECTIVE IV)

Objectives:

To enable the students

1. *To understand different commercially available PLDS, FPGAs.*
2. *To understand different architectures and routing technology in CPLDS and FPGAs.*
3. *To understand* FSM architectures and systems level design.
4. *To familiarize with frontend and backend design tools.*

Outcomes:

The student will

1. *know about different commercially available FPGA and CPLD architectures.*
2. *design logic blocks using optimization techniques.*
3. *Understand the top down design of digital circuits.*
4. *know about mentor graphics EDA tool.*

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for FPGAs.

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs, Problem of Initial State Assignment for One Hot Encoding. **REALIZATION OF STATE MACHINE:** Charts with a PAL, Alternative Realization for State Machine Chart using Micro-programming, Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT VI

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered around Non-Registered PLDs, State Machine Designs Centered around Shift Registers, One – Hot Design Method, Use of ASMs in One – Hot Design, K Application of One – Hot Method, System Level Design – Controller, Data Path and Functional Partition.

UNIT V

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Parallel Adder Cell, Parallel Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS:

1. P.K.Chan& S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall , 1994.
2. Stephen M Trimberger, "Field Programmable Gate Array Technology", Springer international Edition, 2007.
3. Stephen D Brown, R.Francis, J.Rose, Z.Vranesic, "Field Programmable Gate Array", Springer, 1992.

REFERENCES:

1. J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley & Sons,2008.
2. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, Newnes,2008.

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

	L	T	P	C
M.Tech-II Semester- EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BVL13) NANO ELECTRONICS
(ELECTIVE IV)

Objectives:

To enable the students

1. *To understand carbon based nano structures and their properties and application*
2. *To understand the fabrication of nano films with various methods*
3. *To understand the carbon based devices.*
4. *To understand how nano electronic devices can be used in electronic applications such as logic memory & mass storage devices..*

Outcomes:

On completion of course The student will be able

1. *To understand various methods to fabricate.*
2. *To measure nano scale features*
3. *To attain knowledge mass storage device*
4. *To understand data transmission*

UNIT I

NANO TECHNOLOGY AND SCIENCE:

Introduction, Nano film deposition techniques, Magnetron sputtering, Laser Ablation, Molecular beam epitaxy deposition, Lithography, Material Removing Technologies, Chemical Etching , Mechanical Processing, Scanning Probe Techniques. Carbon nano structures: C_{60} and Fullerence, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II

LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III

RADOM ACESS MEMORIES: High Permitivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT IV

MASS STORAGE DEVICES:

Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V

DATA TRANSIMISSION, INTERFACES AND DISPLAYS:

Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:

1. Rainer Waser, "Nano Electronics and Information Technology", Wiley VCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Inter science, May 2003

Reference Books:

1. George W. Hanson, "Fundamentals of Nano electronics", 2009
2. Mitin, "Introduction To Nano electronics Science, Nanotechnology, Engineering, And Applications", 2010

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

(15BDE15) HIGH SPEED NETWORKS
(ELECTIVE-IV)

Objectives:

1. will get an introduction about ATM and Frame relay.
2. will be provided with an up-to-date survey of developments in High Speed Networks.
3. to know techniques involved to support real-time traffic and congestion control.
4. will be provided with different levels of quality of service to different applications.

Outcomes:

After completion of this course the student will be able to:

1. Design the different technologies involved in High Speed Networking and their performance.
2. Understand switching in ATM and Frame Relay networks.
3. Develop an in-depth understanding, in terms of architecture, protocols and applications of major high-speed networking technologies.
4. Solve numerical or analytical problems pertaining to the high-speed networking technologies.

UNIT I

NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture, QOS in IP networks: differentiated and integrated services.

UNIT II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III

ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections, QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT IV

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage class networks.
REARRANGEABLE NETWORKS: Rearrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT V

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.
TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active.

TEXT BOOKS:

1. William Stallings, "ISDN & B-ISDN with Frame Relay", PHI.
2. Leon Garcia widjaja, "Communication Networks", TMH, 2000.
3. N. N. Biswas, "ATM Fundamentals", Adventure books publishers.

Reference Books:

1. Warland & Pravin Varaiya," HIGHPER FOR MANCE COMMUNICATION NETWORKS", JeanHardcourt Asia Pvt. Ltd., II Edition,2001.
2.William Stallings, "HIGH SPEED NETWORKS AND INTERNET", Pearson Education, Second Edition, 2002.
3.Abhijit S. Pandya, Ercan Sea, "ATM Technology for Broad Band Telecommunication Networks", CRC Press, New York, 2004.

Sri Venkateswara College of Engineering and Technology, Chittoor.
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M.Tech - II Semester-EMBEDDED SYSTEMS	**0**	**0**	**3**	**2**

(15BEM09) - RTOS & FPGA LAB

Objectives:

To enable the students

1. to design of combinational circuits and sequential circuits.
2. to Understand simulation and synthesize of digital circuits.

Outcomes:

After completion of course

1. Students are able to simulate and synthesize combinational circuits.
2. Students are able to simulate and synthesize sequential circuits.

1. RTOS System solution & tools

2. Testing RTOS Environment and System Programming.

   a) Keil Tools

   b) RTOS System Solutions with Tornado tools.

3. Embedded DSP based System Designing.

   a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.

   b) Analog DSP tool kit.

4. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after Simulation are to be verified using FPGA/CPLD blocks from different commercially available products on:

a). Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)

b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

NOTE: Required Software Tools for FPGA:

1**.** Mentor Graphic tools / Cadence tools/ Synopsis tools. (220 nm Technology and Above)

2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

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M.Tech- II Semester-EMBEDDED SYSTEMS	**0**	**0**	**3**	**2**

(15BDE18) - ADVANCED DSP LAB

Objectives:

To enable the students

1. To familiarize with CC Studio and DSP starter kit.
2. To design a FIR filter and IIR filter.
3. To implement FIR filter and IIR filter on DSP trainer kit.
4. To calculate power spectrum using various methods.

Outcomes:

After completion of course

1. Students are able to implement FIR and IIR filters on DSP trainer kit.
2. Students are able to estimate power spectrum using various methods.
3. Students are able to implement DIT and DIF algorithms using CC Studio.

Note: Minimum 12 experiments are to be conducted

1. FIR Filter design Using Matlab
2. IIR Filter design Using Matlab
3. DIT-FFT Algorithm using CC Studio
4. DIF-FFT Algorithm using CC Studio
5. FFT of 1-D Signal using CC Studio
6. Power Density Spectrum of given Sequence using CC Studio
7. Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
8. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code)
9. Program to verify Decimation and Interpolation of a given Sequences.
10. Plot the Periodogram of a Noisy Signal and estimate PSD using Periodogram and Modified Periodogram methods
11. Estimation of Power Spectrum using Bartlett and Welch methods
12. Verification of Autocorrelation Theorem
13. Parametric methods (Yule-Walker and Burg) of Power Spectrum Estimation
14. Generation of Dual Tone Multiple Frequency (DTMF) Signals

Note: Use MATLAB and DSP Processor Kits.

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M.Tech- II Semester-EMBEDDED SYSTEM	**0**	**0**	**0**	**2**

(15BEM10) SEMINAR - II

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	L	T	P	C
M.Tech- II Semester-EMBEDDED SYSTEM	**0**	**0**	**0**	**2**

(15BEM11)COMPREHENSIVE VIVA

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	L	T	P	C
M.Tech- II YEAR III & IV SEMESTERS - EMBEDDED SYSTEMS	**0**	**0**	**0**	**12**

(15BEM12) PROJECT WORK