SRI VENKATESWARA COLLEGE OF ENGINNERING & TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTAPUR)
ACADEMIC REGULATIONS
M.TECH REGULAR 2 YEAR DEGREE PROGRAMME
(FOR THE BATCHES ADMITTED FROM THE ACADEMIC YEAR 2015-16)

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time. Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE/PGECET score, subject to reservations and policies prescribed by the Government from time to time.

2.0 ADMISSION PROCEDURE:

As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows:

a) Category –A seats are to be filled by Convenor through PGECET/GATE score.

b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A.P.

3.0 Specializations:

Sl. No	Department	Specializations
1.	CE	Structural Engg.
2.	EEE	Power Electronics & Electrical Drives
3.	EEE	Electrical Power Systems
4.	ME	CAD/CAM
5.	ME	Machine Design
6.	ECE	VLSI System Design
7.	ECE	Digital Electronics and Communication System
8.	ECE	Embedded systems
9.	CSE	Computer Science & Engg.
10.	CSE	Computer Science
11.	IT	Software Engg.

4.0 COURSE WORK:

4.1. A Candidate after securing admission must pursue the M.Tech course of study for Four Semesters duration.

4.2. Each semester shall have a minimum of 16 instructional weeks.

4.3. A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

5.0 ATTENDANCE:

5.1. A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance on cumulative basis of all subjects/courses in the semester.

5.2. Condonation of shortage of attendance up to 10% i.e., from 65% and above and less than 75% may be given by the college on the recommendation of the Principal.

5.3. Condonation of shortage of attendance shall be granted only on medical grounds and on representation by the candidate with supporting evidence.

5.4. If the candidate does not satisfy the attendance requirement he is detained for want of attendance and shall reregister for that semester. He shall not be promoted to the next semester.

6.0 EVALUATION:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practical's, on the basis of Internal Evaluation and End Semester Examination.

6.1. For the theory subjects 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation, based on the average of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (first two units) and another immediately after the completion of instruction (last three units) with four questions to be answered out of five in 2 hours, evaluated for 40 marks. For semester end examination (external paper setting & external evaluation) five questions shall be given for a maximum of 60 marks with one question from each unit with internal choice i.e. either or type. All questions carry equal marks.

6.2. For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance (25 marks) and practical test at the end of the semester (15 marks).

6.3. Seminar is a continuous assessment process. For Seminar there will be an internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts.

6.4. For comprehensive viva voce there will be an internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts.

6.5. A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

6.6. In case the candidate does not secure the minimum academic requirement in any of the subjects (as specified in 6.5) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the subject when next offered or do any other specified subject as may be required.

6.7. **Revaluation / Recounting:**

Students shall be permitted for request for recounting/revaluation of the Semester-End examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised grade sheet. If there are no changes, the same will be intimated to the students.

6.8**. Supplementary Examination:**

In addition to the regular Semester- End examinations conducted, the College may also schedule and conduct supplementary examinations for all the subjects of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

7.0 RE-REGISTRATION:

Following are the conditions to avail the benefit of improvement of internal evaluation marks

7.1. The candidate should have completed the course work and obtained examinations results for I & II semesters.

7.2. He should have passed all the subjects for which the Internal evaluation marks secured are more than or equal to 50%.

7.3. Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

7.4. The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

7.5. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the along with the requisition to the Principal of the college.

7.6. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

8.0 EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ institute.

8.1. Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of I & II Semesters.

8.2. An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor and one internal senior teacher shall monitor the progress of the project work.

8.3. The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4. The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report and award internal assessment marks for 120.

8.5. A candidate shall be allowed to submit the Thesis / Dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva voce examination may be conducted once in two months for all the candidates who have submitted thesis during that period.

8.6. Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor and HOD shall be presented to the H.OD. One copy is to be forwarded to the Controller Of Examinations and one copy to be sent to the examiner.

8.7. The Dept shall submit a panel of three experts for a maximum of 5 students at a time. However, the Thesis / Dissertation will be adjudicated by one examiner nominated by the Chief Controller Of Examinations.

8.8. If the report of the examiner is favorable viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis / dissertation. The board shall jointly award the marks for 180.

8.9. A candidate shall be deemed to have secured the minimum academic requirement in the project work if he secures a minimum of 50% marks in the end viva-voce examination and a minimum aggregate of 50% of the total marks in the end viva-voce examination and the internal project report taken together. If he fails to get the minimum academic requirement he has to appear for the viva-voce examination again to get the minimum marks. If he fails to get the minimum marks at the second viva-voce examination he will not be eligible for the award of the degree, unless the candidate is asked to revise and resubmit. If the candidate fails to secure minimum marks again, the project shall be summarily rejected.

9.0 Grades, Grade point Average, Cumulative Grade point Average:

9.1. Grade System: After all the components and sub-components of any subject (including laboratory subjects) are evaluated, the final total marks obtained will be converted to letter grades on a "10 point scale" described below.

% of marks obtained	Grade	Grade Points(GP)
90 to 100	A+	10
80 to 89	A	9
70 to 79	B	8
60 to 69	C	7
50 to 59	D	6
Less than 50 in sum of Int. and Ext. (or) Less than 40 in Ext.	F	0
Not Appeared	N	0

9.2. GPA: Grade Point Average (GPA) will be calculated as given below on a "10 Point scale" as an Index of the student's performance at the end of each semester:

$$\textbf{GPA} = \frac{\sum(CXGP)}{\sum C}$$

Where C denotes the credits assigned to the subjects undertaken in that semester and GP denotes the grade points earned by the student in the respective subjects

9.3. CGPA: At the end of every semester, a Cumulative Grade Point Average (CGPA) on a 10 Point scale is computed considering all the subjects passed up to that point as an index of overall Performance up to that Point as given below:

$$\textbf{GPA} = \frac{\sum(CXGP)}{\sum C}$$

Where C denotes the credits assigned to subjects undertaken upto the end of the current semester and GP denotes the grade points earned by the student in the respective courses.

9.4. Grade sheet: A grade sheet (Marks Memorandum) will be issued to each student Indicating his performance in all subjects registered in that semester indicating the GPA and CGPA. GPA and CGPA will be rounded off to the second place of decimal.

9.5 Transcripts: After successful completion of the entire Program of study, a transcript containing performance of all semesters will be issued as a final record. Duplicate transcripts will also be issued, if required, after payment of requisite fee.

10.0 Award of Degree: The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Anantapur on the recommendation of The Principal of SVCET (Autonomous).

10.1 Eligibility: A student shall be eligible for the award of M.Tech. Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the program of study for which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the specialization of study within the stipulated time.
- Obtained CGPA greater than or equal to 6.0 (Minimum requirement for declaring as passed.)

10.1 Award of Class: Declaration of Class is based on CGPA.

Cumulative Grade Point Average	**Class**
≥7.75	First Class with Distinction
≥6.75 and<7.75	First Class
≥6.0 and <6.75	Second Class

11.0 WITHHOLDING OF RESULTS: If the candidate has not paid dues to the university or If any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

12.0 TRANSITORY REGULATIONS*:*

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to 6.5 and 4.3 sections. Whereas they continue to be in the academic regulations of the batch they join later.

13.0 GENERAL:

i. The academic regulations should be read as a whole for purpose of any interpretation.
ii. Disciplinary action for Malpractice/improper conduct in examinations is appended.
iii. Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".
iv. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.
v. The college may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the college.

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Sri Venkateswara College of Engineering And Technology (Autonomous)
R.V.S. Nagar, Chittoor

Identification of Courses

M. Tech

Each course shall be uniquely identified by an alphanumeric code of width 7 characters as given below.

No. of digits	Description
First two digits	Year of regulations Ex:15
Next one letter	Type of program: A: B. Tech B: M. Tech C: M.B.A D: M.C.A
Next two letters	Code of program: ST: Structural Engineering, P.E: Power Electronics & Electric Drives, PS: Electrical Power Systems, CM: CAD/CAM, MD: Machine Design, VL: VLSI, DE: DECS, EM: Embedded Systems, CS: Computer Science and Engineering, CO: Computer Science, SE: Software Engineering,
Last two digits	Indicate serial numbers: ≥ 01

Ex:

15BST01

15BPE01

15BPS01

15BCM01

15BMD01

15BVL01

15BDE01

15BEM01

15BCS01

15BCO01

15BSE01

SRI VENKATESWARA COLLEGE OF ENGINNERING & TECHNOLOGY
(AUTONOMOUS)
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RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices / Improper conduct	**Punishment**
	If the candidate	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.

3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred and forfeits of seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.

8.	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction or property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.

10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

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Course Structure and Syllabi for M. Tech in Digital Electronics & Communication Systems

M.Tech I year I Semester

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BDE01	Digital System Design	3	1	-	4	40	60	100
2	15BDE02	Advanced Digital Signal Processing	3	1	-	4	40	60	100
3	15BEM02	Embedded System Design	3	1	-	4	40	60	100
4	15BDE03	Digital Communication Techniques	3	1	-	4	40	60	100
		Elective-I:							
5	15BCS11	1. Advanced Computer Architecture	3	1	-	4	40	60	100
6	15BDE04	2. Optical Communication Networks							
7	15BVL01	3. VLSI Technology							
		Elective-II:							
8	15BCS19	1. Cloud Computing	3	1	-	4	40	60	100
9	15BDE05	2. Adaptive Signal Processing							
10	15BDE06	3. Image Processing and Pattern Recognition							
11	15BDE07	Digital System Design Lab	-	-	3	2	40	60	100
12	15BEM05	Embedded Systems Lab	-	-	3	2	40	60	100
13	15BDE08	Seminar-I	-	-	-	2	50	-	50
		TOTAL:	**18**	**6**	**6**	**30**	**370**	**480**	**850**

M.Tech I Year II Semester

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BDE09	Wireless Communications	3	1	-	4	40	60	100
2	15BDE10	Coding Theory and Techniques	3	1	-	4	40	60	100
3	15BDE11	DSP Processors and Architectures	3	1	-	4	40	60	100
4	15BDE12	Detection and Estimation of Signals	3	1	-	4	40	60	100
		Elective III :							
5	15BDE13	1.Compression Techniques	3	1	-	4	40	60	100
6	15BDE14	2. Micro Computer System Design							
7	15BVL13	3. Nano Electronics							
		Elective IV:							
8	15BDE15	1. High Speed Networks	3	1	-	4	40	60	100
9	15BVL09	2. FPGA Architectures and Applications							
10	15BDE16	3. Neural Networks and Fuzzy Logic							
11	15BDE17	Advanced Communications Lab	-	-	3	2	40	60	100
12	15BDE18	Advanced DSP Lab	-	-	3	2	40	60	100
13	15BDE19	Seminar-II	-	-	-	2	50	-	50
14	15BDE20	Comprehensive viva	-	-	-	2	100	-	100
		TOTAL:	**18**	**6**	**6**	**32**	**470**	**480**	**950**

M.Tech II Year III & IV Semesters

Sl. No.	Course Code	Subject	Periods			Credits	Scheme of Examination (Maximum Marks)		
			L	T	P		Internal	External	Total
1	15BDE21	Project Work	-	-	-	12	120	180	300

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M.Tech- I Semester-DECS	**L**	**T**	**P**	**C**
	3	**1**	**0**	**4**

(15BDE01) DIGITAL SYSTEM DESIGN

Objectives:

Students are able to

1. *Know different Hardware description languages.*
2. *Understand fault classes and fault models of the digital circuits.*
3. *Know test pattern generation techniques and algorithms.*
4. *Understand optimization techniques in Programmable logic arrays*

Outcomes:

After completion of the course, the students will

1. *able to design digital circuit using different levels of modeling in HDL.*
2. *able to fault model digital circuits*
3. *familiarze different commercially available PLDs.*
4. *able to design optimized programmable logic arrays*

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT II

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature Analysis and testing for bridging faults.

UNIT III

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

UNIT IV

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT V

ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCES:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications.
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4^{th} Edition.

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	L	T	P	C
M.Tech-I Semester-DECS	**3**	**1**	**0**	**4**

(15BDE02) ADVANCED DIGITAL SIGNAL PROCESSING

Objectives:

To enable the students

1. *To understand the fast Fourier transform algorithms.*
2. *To understand the design of digital filters.*
3. *To understand the multirate signal processing.*
4. *To understand the finite word length effects in digital filters.*

Outcomes:

The student will

1. *Know the fundamentals of Discrete time Systems.*
2. *have knowledge on the Realization of digital filters.*
3. *have knowledge on implementation of sampling rate conversion.*
4. *familiar with the various Applications of Digital Signal Processing.*

UNIT I

OVERVIEW Discrete-Time Signals, Sequences and sequence Representation, Discrete-Time Systems, Time-Domain Characterization and Classification of LTI Discrete-Time Systems. The Continuous-Time Fourier Transform, The discrete-Time Fourier Transform, energy Density Spectrum of a Discrete-Time Sequence, Band-Limited Discrete-Time signals, The Frequency Response of LTI Discrete-Time System.

DSP ALGORITHEMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform

UNIT II

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

DIGITAL FILTER SRTUCTURE AND DESIGN: All Pass Filters, Tunable IIR Digital Filter, IIR Tapped Cascade Lattice Structures, FIR Cascaded Lattice Structures, Parallel All Pass Realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine-Cosine Generator, Computational Complexity of Digital Filter Structures, Design of IIR Filter using pade' approximation, Least Square Design Methods, Design of Computationally Efficient FIR Filters.

UNIT III

MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

ANALYSIS OF FINITE WORDLENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality-Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT IV

POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT V

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Non stationary Signals, Musial Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete-Time Analytic Signal Generation.

TEXTBOOKS:

1. Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications.
2. Digital Signal Processing Principles, Algorithms, Applications by J G Proakis, D G Manolokis, PHI.

REFERENCES:

1. Discrete-Time Signal Processing by A V Oppenhiem, R W Schafer, Pearson Education.
2. DSP- A Practical Approach- Emmanuel C Ifeacher Barrie. W. Jervis, Pearson Education.
3. Modern spectral Estimation techniques by S. M .Kay, PHI, 1997.

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	L	T	P	C
M.Tech- I Semester- DECS	**3**	**1**	**0**	**4**

(15BEM02) EMBEDDED SYSTEM DESIGN

Objectives:

1.To study the overview of embedded system.

2.To know various communication interfacings.

3.To study the scheduling architectures

4.To study the ARM and SHARC processor.

Outcomes:

After the completion of the course,the students will be able :

1. to perform system analysis and architecture design

2. to apply embedded concepts on real time applications

3. to get knowledge on ARM processor and SHARC processor

4. to get an idea about Debugging techniques

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT III

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT IV

INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002.

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	L	T	P	C
M.Tech-ISemester-DECS	**3**	**1**	**0**	**4**

(15BDE03) DIGITAL COMMUNICATION TECHNIQUES

Objectives:

1.Iintroduction to random variables and processes.

2.Tto distinguish between signal and vector space concepts.

3.To study the communication over Additive Gaussian noise channels

4. To study the communication over fading channels

Outcomes:

After completion of the course, the students will able:

1. To understand the signal space and vector space representation.

2. To find out the error probabilities in receiver

3. To understand the performance of various digital modulation schemes

4. To understand OFDM technique.

UNIT I

REVIEW OF RANDOM VARIABLES AND PROCESSES: Random variable – Moment generating function – Markov's inequality – Chebyshev's inequality – Central limit theorem – Chi square, Rayleigh, and Ricean distributions – Correlation – Covariance matrix – Stationary processes – Wide sense stationary processes – Ergodic process – Cross correlation – Autocorrelation functions – Gaussian process.

UNIT II

CHARACTERIZATION OF COMMUNICATION SIGNALS AND SYSTEMS: Signal space representations- Vector Space Concepts, Signal Space Concepts, Orthogonal Expansion of Signals. Representation of Digitally Modulated Signals- Memory less Modulation Methods.

UNIT III

COMMUNICATION OVER ADDITIVE GAUSSIAN NOISE CHANNELS - I: Optimum waveform Receiver in additive white Gaussian noise (AWGN) channels, Cross correlation receiver, Matched Filter receiver and error probabilities.

COMMUNICATION OVER ADDITIVE GAUSSIAN NOISE CHANNELS - II: Optimum receiver for signals with random phase in AWGN channels, Optimum receiver for binary signals, Optimum receiver for M-ary orthogonal signals, Probability of error for envelope detection of M-ary orthogonal signals. Optimum waveform receiver for colored Gaussian noise channels, Karhunen Loeve expansion approach, whitening.

UNIT IV

DIGITAL COMMUNICATION OVER FADING CHANNELS: Optimum coherent and non-coherent receiver in random amplitude, random phase channels- Performance of Rayleigh and Ricean channels, Performance of digital Modulation schemes such as BPSK, QPSK, FSK, DPSK, MSK etc. over wireless channels.

UNIT V

COMMUNICATION OVER BAND LIMITED CHANNELS: Communication over band limited Channels- Optimum pulse shaping- Nyquist criterion for zero ISI, partial response signaling- Equalization Techniques, Zero forcing linear Equalization- Decision feedback equalization.

ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (OFDM): Carrier Synchronization, Timing synchronization, Multichannel and Multicarrier Systems.

TEXT BOOKS:

1. J. Proakis, Digital Communications, McGraw Hill, 2000
2. J. Viterbi and J. K. Omura, Principles of Digital Communications and Coding, McGraw Hill, 1979
3. Andrew J Viterbi, CDMA Principles of Spread Spectrum Communications, Addison Wesley, 1995.

REFERENCE BOOKS:

1. Ahmad R S Bahai ,Burton R Saltzberg ,Mustafa Ergen, "Multi-carrier Digital Communications: Theory and Applications of OFDM." Springer Publications.
2. Edward. A. Lee and David. G. Messerschmitt, "Digital Communication", Allied Publishers (second edition).
3. William Feller, "An introduction to Probability Theory and its applications", Vol 11, Wiley 2000.

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	L	T	P	C
M.Tech- I Semester-DECS	**3**	**1**	**0**	**4**

(15BCS11) ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE-I)

Objectives:

The objective of this course is to make students to:

1. *Acquire the knowledge of machine level representation of data, assembly level organization, memory system organization and architecture, system connection, memory, input/output, instruction sets, CPU structure and functions and the control Unit operation.*
2. *To provide in-depth coverage of current and emerging trends in computer architectures, focusing on performance and the hardware/software interface.*
3. *Acquire the knowledge of computer organization and architecture (logical design) and relates this to contemporary design issues*

Outcomes:

At the end of the course *the student will be able to:*

1. *Understand memory hierarchy and its impact on computer cost/ performance.*
2. *Obtain technical knowhow of the advantage of instruction level parallelism and pipelining for high performance processor design.*
3. *Design key features of advanced processing and memory systems.*
4. *Develop solutions to computing problems using alternative architectures*.

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III

INSTRUCTION LEVEL PARALLELISM (ILP): overc oming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP.

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT IV

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT V

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1. John. Hennessy & David A. Patterson Morgan Kufmann, "Computer Architecture A quantitative approach", 3rd edition (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A. Briggs, "Computer Architecture and parallel Processing", International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

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	L	T	P	C
M.Tech-ISemester-DECS	**3**	**1**	**0**	**4**

(15BDE04) OPTICAL COMMUNICATION NETWORKS
(ELECTIVE-I)

Objective:

1. To learn the concepts of fiber mechanical characterization of fibers, optical cable design
2. To make the students learn the system with various components or process for various applications.
3. To enlighten the student with latest trends in optical communications.
4. To introduce various signal degradation factors associated with optical fiber.

Outcome:

Student will be able to

1. Design an optical fiber communication link with various optical fiber techniques
2. Measure the characteristics of LED, LASER source and Photo detectors.
3. Measure dispersion and attenuation in OFC.
4. Familiarized with access network, soliton communication

UNIT I

INTRODUCTION: Evolution of fiber types, guiding properties of fibers, cross talk between fibers, coupled modes and mode mixing, dispersion properties of fibers, nonlinear properties of optical fibers, SRS, SBS, intensity dependent refractive index; Fiber design considerations: diameter, cladding, thickness, low and high bit rate systems, characterization of materials for fibers, fiber perform preparation, fiber drawing and control, roles of coating and jacketing;

UNIT II

OPTICAL AND MECHANICAL CHARACTERIZATION OF FIBERS, OPTICAL CABLE DESIGN: Design objectives and cable structures, fiber splicing, fiber end preparation, single and array splices, measurement of splicing efficiency, optical fiber connectors, connector alignments, optical sources for communication, LED, injection lasers, modulation technique, direct and indirect methods, optical waveguide devices

OPTICAL DETECTORS: Photodiodes in repeaters, receiver design, digital and analog, transmission system design, system design choices, passive and low speed active optical components for fiber system, micro-optic components, lens-less components.

UNIT III

OPTICAL FIBER COMPONENTS: couplers, Isolators and Circulators, Multiplexers, Bragg grating, Fabry-perot Filters, Mach zender interfermometers, Arrayed waveguide grating, tunable filters, hi-channel count multiplexer architectures, optical amplifiers, direct and external modulation transmitters, pump sources for amplifiers, optical switching and wave length converters.

UNIT IV

OPTICAL FIBER TECHNIQUES-1: Modulation and demodulation, signal formats, direction detection receivers, coherent detection.

OPTICAL FIBER TECHNIQUES-2: Optical switching, polarization control, inter office transmission system, trunking system, performance and architecture, under sea cable system, optical fibers in loop distribution system, photonic local network.

UNIT V

ACCESS NETWORK: Network architecture, HFC, FTTC, optical access network architecture, deployment considerations, upgrading the transmission capacity, SDM, TDM, WDM, application areas, inter exchange, undersea, local exchange networks; Packaging and cabling of photonics components- photonic packet switching, OTDM, multiplexing and de-multiplexing, optical logic gates, synchronization, broadcast OTDM network, OTDM test beds.

SOLITON COMMUNICATION: Basic principle, metropolitan optical network, cable TV network, optical access network, photonics simulation tools, error control coding techniques, nonlinear optical effects in WDM transmission.

TEXT BOOKS:

1. Gil Held, "Deploying Optical Network Components".
2. Gerd Kaiser, "Optical Fiber Communication", McGraw Hill.
3. Rajiv Ramaswamy and Kumar and N. Sivaranjan, "Optical Networks".

REFERENCES:

1. S E Miller, A G Chynoweth, "Optical Fiber Telecommunication".
2. S E Miller, I Kaninov, "Optical Fiber Telecommunication II".
3. John. M. Senior, "Optical fiber communications: Principles and Practice".

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	L	T	P	C
M.Tech -I Semester- DECS	**3**	**1**	**0**	**4**

(15BVL01) VLSI TECHNOLOGY
(ELECTIVE-I)

Objectives:

1. *To introduce basic NMOS, CMOS & Bi-CMOS logic.*
2. *To study electrical properties of MOS devices.*
3. *To understand the design of Low power gates*.
4. *To analyze the combinational and sequential* system design

Outcomes:

After completion of the course, the student will

1. *Gain knowledge of different VLSI fabrication processes and CMOS Logic Design.*
2. *be able to Design different MOS logical circuits.*
3. *be able to know the various tools in the layout analysis*
4. *be able to know about Floor planning methods.*

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: I_{ds} -V_{ds} Relationships, Threshold Voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT IV

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNITV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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	L	T	P	C
M.Tech -I Semester- DECS	**3**	**1**	**0**	**4**

(15BCS19) CLOUD COMPUTING
(ELECTIVE-II)

Objectives:

The Objective of this course is to make students to

1 *Learn fundamental ideas behind Cloud Computing, the evolution of the paradigm, its applicability; benefits, as well as current and future challenges;*
2 *Learn about cloud storage technologies and relevant distributed file systems;*
3 Understand the emerging area of "cloud computing" and how it relates to traditional models of computing.
4 Gain competence in Map Reduce as a programming model for distributed processing of large datasets.

Outcomes:

At the end of course student should be able to

1 Articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art cloud computing
2 Identify the architecture and infrastructure of cloud computing, including SaaS, PaaS, IaaS, public cloud, private cloud, hybrid cloud, etc.
3 Explain the core issues of cloud computing such as security, privacy, and interoperability.
4 Choose the appropriate technologies, algorithms, and approaches for the related issues.

UNIT I

Overview of Cloud Computing: Meaning of the terms cloud and cloud computing, cloud based service offerings, Grid computing vs Cloud computing, Benefits of cloud model, limitations, legal issues, Key characteristics of cloud computing, Challenges for the cloud, The evolution of cloud computing.

UNIT II

Web services delivered from the cloud: Infrastructure as a service, Platform-as-a-service, Software-as-a-service. Building Cloud networks: Evolution from the MSP model to cloud computing and software -as-a-service, The cloud data center, SOA as step toward cloud computing, Basic approach to a data center based SOA.

UNIT III

Federation Presence, Identity and Privacy in the cloud: Federation in the cloud, Presence in the cloud, Privacy and its relation to cloud based information system. Security in the Cloud: Cloud security challenges, Software-as-a-service security, Common Standards in Cloud computing: The open cloud consortium, The distributed management task force, standards for application developers, standards for messaging, standards for security.

UNIT IV

End user access to cloud computing: youtube, zimbra, Facebook, Zoho, DimDim Collaboration Mobile internet devices and the cloud: Smartphone, mobile operating systems for smart phones, Mobile Platform virtualization, Collaboration applications for mobile platforms, Future trends.

UNIT V

Virtualization: Adding guest Operating system. Cloud computing, Downloading open Solaris as a Guest OS, Using the 7-Zip Archive Tool casestudies1: Amazon EC2, Amazon simple DB,: Google App Engine.

TEXT BOOKS:

1. John W. Rittinghouse, James F. Ransome ,"*Cloud Computing implementation, management and security*", CRC Press, Taylor &Francis group, 2010.
2. Anthony T.velte, TobJ.velte Robert Elsenpeter, "*Cloud Computing: A practical approach*", Tata McGraw Hill edition, 2010.

REFERENCES:

1. George Reese, *Cloud Application Architectures Building Applications and Infrastructure in the Cloud*, O'Reilly Media Released, April 2009.
2. David S. Linthicum ,"*Cloud Computing and SOA convergence in your enterprise*", Addison-Wesley.

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	L	T	P	C
M.Tech-I Semester-DECS	**3**	**1**	**0**	**4**

(15BDE05) ADAPTIVE SIGNAL PROCESSING
(ELECTIVE – II)

Objectives:

1.To understand the properties of eigen values.

2.To understand the development of adaptive filter theory .

3.To study the various adaptive algorithms and applications.

4.To understand the non linear adaptive filtering .

Outcomes:

After completion of the course, the student will

1. able to familiarize with adaptive system.

2. able to familiarize with Gradient searching algorithms.

3. able to familiarize with the various applications of adaptive filters.

4. able to familiarize with the Kalman filtering and Extend Kalman filtering.

UNIT I

EIGEN ANALYSIS: Eigen Value Problem, Properties of eigen values and eigen vectors, Eigen Filters, eigen Value computations.

INTRODUCTION TO ADAPTIVE SYSTEMS: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description, Weight Vectors, Desired Response Performance function, Gradient & Mean Square Error.

UNIT II

DEVELOPMENT OF ADAPTIVE FILTER THEORY & SEARCHING THE PERFORMANCE SURFACE: Introduction to Filtering, Smoothing and Prediction, Linear Optimum Filtering, Problem statement, Principle of Orthogonality - Minimum Mean Square Error, Wiener- Hopf equations, Error Performance - Minimum Mean Square Error.

SEARCHING THE PERFORMANCE SURFACE – Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability & Rate of convergence - Learning Curves.

UNIT III

STEEPEST DESCENT ALGORITHMS: Gradient Search by Newton's Method, Method of Steepest Descent, Comparison of Learning Curves.

LMS ALGORITHM & APPLICATIONS: Overview - LMS Adaptation algorithms, Stability & Performance analysis of LMS Algorithms - LMS Gradient & Stochastic algorithms, Convergence of LMS algorithm.

Applications: Noise cancellation, Cancellation of Echoes in long distance telephone circuits, Adaptive Beam forming.

UNIT-IV

RLS ALGORITHM: Matrix Inversion lemma, Exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, convergence analysis of RLS Algorithm, Application of RLS algorithm on Adaptive Equalization

UNIT V

KALMAN FILTERING: Introduction, Recursive Mean Square Estimation Random variables, Statement of Kalman filtering problem, Filtering, Initial conditions, Variants of Kalman filtering, Extend Kalman filtering.

NON LINEAR ADAPTIVE FILTERING: Theoretical and Practical considerations of Blind Deconvolution, Buss Gang Algorithm for blind Equalization of real base band Channels.

TEXT BOOKS:

1. Adaptive Signal Processing - Bernard Widrow, Samuel D.Strearns, 2005, PE.
2. Adaptive Filter Theory - Simon Haykin-, 4 ed., 2002,PE Asia.

REFERENCES:

1. Optimum signal processing: An introduction - Sophocles.J.Orfamadis, 2 ed., 1988, McGraw-Hill, New york
2. Adaptive signal processing-Theory and Applications, S.Thomas Alexander, 1986, Springer –Verlag.

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	L	T	P	C
M.Tech-I Semester-DECS	**3**	**1**	**0**	**4**

(15BDE06) IMAGE PROCESSING AND PATTERN RECOGNITION
(ELECTIVE – II)

Objectives:

1. *To understand the general processes of image acquisition, storage, enhancement, segmentation, representation and description.*
2. *To implement filtering and enhancement algorithms for monochrome as well as color images.*
3. *To aware the challenges and understand the principles and applications of visual pattern recognition.*
4. *To Know various techniques of Image Processing And Pattern Recognition*

Outcomes:

After completion of the course, the student will

1. *The student will be able to describe and explain the general processes of image acquisition and storage.*
2. *The student will be able to do enhancement, segmentation, representation, and description.*
3. *The student will be able to implement filtering and enhancement algorithms for monochrome as well as color images.*
4. *The student will learn be able to design and implement visual pattern recognition solutions.*

UNIT I

Image representation: Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II

Image enhancement: Filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge detection, non parametric and model based approaches, LOG filters, localization problem.

Image Restoration: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT III

Image Segmentation: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Edge detection, Hough transform, Region growing.

Fundamental concepts of image compression: Compression models, Information theoretic perspective, Fundamental coding theorem.

UNIT IV

INTRODUCTION: Machine Perception Pattern Recognition Example, Pattern Recognition Systems, The Design Cycle, Learning And Adaption.

Bayesian Decision Theory: Introduction, continuous features – two categories classifications, minimum error-rate classification-zone-one loss function, classifiers, discriminate functions, and decision surfaces.

UNIT V

NORMAL DENSITY: Univariate and Multivariate Density, discriminant functions for the normal density different cases, Bayes decision theory – discrete features, compound Bayesian decision theory and context.

MAXIMUM LIKELIHOOD AND BAYESIAN PARAMETER ESTIMATION: Introduction, maximum likelihood estimation, Bayesian estimation, Bayesian parameter estimation – Gaussian case.

Text BOOKs

1.R. C. Gonzalez, R. E. Woods,"Digital Image Processing", Pearson Education. 2nd edition,2002

2**.** Pattern classifications, Richard O. Duda, Peter E. hart, David G. Stroke. Wiley student edition, Second Edition.

3.Pattern Recognition, Third Edition, by Sergios Theodoridis and Knostantinos koutroumbas, Academic press.

References:

1. *S jayaraman, S Esakkirajan, T Veerakumar, "Digital Image processing",Tata McGraw Hill*
2. R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw-Hill International Edition, 1995
3. Fundamentals of Speech Recognition, Lawerence Rabiner, Biing – Hwang Juang Pearson education.

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	L	T	P	C
M.Tech-I Semester-DECS	**0**	**0**	**3**	**2**

(15BDE07) DIGITAL SYSTEM DESIGN LAB

Objectives:

1. To Verify the Functionality of Designed digital circuits .
2. To synthesis and verify timing synthesis of digital circuits.

Outcomes:

After completion of the lab students will be able to:

1. Know the various design methodologies of digital circuits.
2. Know the importance of simulation and synthesis

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.
3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.
4. Modeling of Flip-Flops with Synchronous and Asynchronous reset.
5. Design and Simulation of Counters- Ring Counter, Johnson Counter, and Up- Down Counter, Ripple Counter.
6. Design of a N- bit Register of Serial-in Serial-out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
8. 4- Bit Multiplier, Divider. (for 4-Bit Operand)
9. Design ALU to Perform – ADD, SUB, AND-OR, 1's and 2's COMPLIMENT, Multiplication, Division.

CYCLE 2:

After Digital Circuit Description Using Verilog/ VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Synthesis of Digital Circuit.
4. Place and Router Techniques for FPGA's like Xilinx, Altera, Cypress, etc.,
5. Implementation of Design using FPGA and CPLD Devices.

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	L	T	P	C
M.Tech- I Semester- DECS	**0**	**0**	**3**	**2**

(15BEM05) Embedded Systems Lab

Objectives:

1. To enable the students to program the 8051 and their interfaces

2. To enable the students to program various devices using KIEL

3. To provide a platform for the students to do multidisciplinary projects

Outcomes:

After completion of the course, the students will able:

1.To perform interfacing using LED &LCD.

2. To perform the program using assembly & C Languages.

3. To perform serial transmission& Reception.

ASSEMBLY:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2**.** A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7**.** Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.

3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.

4. LED'S
   (A) Blinking led
   (B) Dancing led's

5. LCD interface

6. Serial Communication
   A) Serial Transmission
   B) Serial Reception

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	L	T	P	C
M.Tech- I Semester- DECS	**0**	**0**	**0**	**2**

(15BDE08) SEMINAR - I

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M.Tech- II Semester-DECS	**L**	**T**	**P**	**C**
	3	**1**	**0**	**4**

(15BDE09) WIRELESS COMMUNICATIONS

Objectives:

To enable the students

1. *To understand the Generations of Wireless Communications.*
2. *To understand the fading and Rayleigh and Ricean Distributions.*
3. *To understand the Diversity techniques.*
4. *To understand the multiple access techniques.*

Outcomes:

The student will be

1. *Understand the Applications Diversity techniques for further studies.*
2. *able to apply different scattering and multi-path fading techniques*
3. *able to know about Maximal length sequences, Gold sequences and their application areas*
4. *know about the Capacity Analysis, Spectral efficiency.*

UNIT I

INTRODUCTION TO WIRELESS COMMUNICATIONS SYSTEMS: Evolution, Examples of Wireless Communication systems, Comparision, Second Generation Cellular Networks, WLL, Bluetooth and Personal Area Networks.

GSM specifications and Air Interface, specifications, IS 95 CDMA- 3G systems: UMTS & CDMA 2000 standards and specifications.

UNIT II

MOBILE RADIO PROPAGATION: Large-Scale Path Loss, Introduction to Radio Wave Propagation, Free Space Propagation Model, Propagation Mechanisms, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering. Small-Scale Fading and Multipath, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-Scale Fading, Rayleigh and Ricean Distributions, Statistical Models for Multipath Fading Channels, Theory of Multipath Shape Factors for Small-Scale Fading Wireless Channels.

UNIT III

DIVERSITY TECHNIQUES: Repetition coding and Time Diversity- Frequency and Space Diversity, Receive Diversity- Concept of diversity branches and signal paths- Combining methods- Selective diversity combining - Switched combining- maximal ratio combining- Equal gain combining- performance analysis for Rayleigh fading channels.

FADING CHANNEL CAPACITY: Capacity of Wireless Channels- Capacity of flat and frequency selective fading channels, Multiple Input Multiple output (MIMO) systems- Narrow band multiple antenna system model, Parallel Decomposition of MIMO Channels- Capacity of MIMO Channels.

UNIT IV

CELLULAR COMMUNICATION: Cellular Networks, Multiple Access: FDM/TDM/FDMA/TDMA, Spatial reuse, Co-channel interference Analysis, Hand over Analysis, Erlang Capacity Analysis, Spectral efficiency and Grade of Service- Improving capacity - Cell splitting and sectorization.

UNIT V

SPREAD SPECTRUM AND CDMA: Motivation- Direct sequence spread spectrum- Frequency Hopping systems, Time Hopping., Anti-jamming- Pseudo Random (PN) sequence, Maximal length sequences, Gold sequences, Generation of PN sequences.

DIVERSITY IN DS-SS SYSTEMS: Rake Receiver- Performance analysis. Spread Spectrum Multiple Access, CDMA Systems- Interference Analysis for Broadcast and Multiple Access Channels, Capacity of cellular CDMA networks- Reverse link power control, Hard and Soft hand off strategies.

TEXT BOOKS:

1. Andrea Goldsmith, "Wireless Communications", Cambridge University press.
2. Simon Haykin and Michael Moher, "Modern Wireless Communications", Person Education.
3. T.S. Rappaport, "Wireless Communication, principles & practice", PHI, 2001.

REFERENCES:

1. G.L Stuber, "Principles of Mobile Communications", 2nd edition, Kluwer Academic Publishers.
2. Kamilo Feher, 'Wireless digital communication', PHI, 1995.
3. R.L Peterson, R.E. Ziemer and David E. Borth, "Introduction to Spread Spectrum Communication", Pearson Education.

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M.Tech-II Semester-DECS

L	T	P	C
3	1	0	4

(15BDE10) CODING THEORY AND TECHNIQUES

Objectives:

To enable the students

1. *To understand the Information theory and their applications.*
2. *To understand the design of Codes to calculate and analyse effciencies.*
3. *To understand the Decoding algorithms.*
4. *To understand the Error Control Coding.*

Outcomes:

The student will

1. *know about the fundamentals of Information theory and applicable areas.*
2. *be able to apply Error Detecting techniques for correcting capability*
3. *analyze different coding and decoding techniques for research purpose.*
4. *Understand the Applications of block, cyclic and BCH codes.*

UNIT I

SOURCE CODING: Mathematical model of Information, Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for Discrete memory less sources, Source coding theorem, Fixed length and Variable length coding, Properties of Prefix codes.

UNIT II

LINEAR BLOCK CODES: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and Correcting capability of Linear Block codes.

UNIT III

Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage systems.

UNIT IV

CYCLIC CODES: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

BCH Codes: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

UNIT V

CONVOLUTIONAL CODES: encoding of Convolutional codes, Structural properties of Convolutional codes, State diagram, Tree diagram, Trellis Diagram, Maximum, Likelihood decoding of Convolutional codes.

Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

TEXT BOOKS:

1. Shulin and Daniel J. Costello, Jr. "Error Control Coding – Fundamentals and Applications", Prentice Hall Inc.
2. Bernard sklar,"Digital Communications – Fundamental and Application", Pearson Education, Asia.
3. Man Young Rhee, "Error Control Coding Theory", McGraw Hill Publ.

REFERENCES:

1. John G. Proakis, "Digital Communications", Mc. Graw Hill Publication.
2. K. Sam Shanmugam, "Digital and Analog Communication Systems", Wiley Publications.
3. Simon Haykin, "Digital Communications", Wiley Publications.

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(Autonomous)	**L**	**T**	**P**	**C**
M.Tech-II Semester-DECS	**3**	**1**	**0**	**4**

(15BDE11) DSP PROCESSORS AND ARCHITECTURES

Objectives:

1. To introduce the basic concepts of DSP
2. To introduce the concepts of DSP Processor and its architectures.
3. To implement the basic DSP algorithms using DSP processor
4. To understand Interfacing memory and I/O devices to programmable DSP devices.

Outcomes:

At the end of this course, the students will be able to understand about the

1. DSP Processors- TMS320C544XX.
2. Implementation of basic DSP algorithms using DSP Processors.
3. Various bus architectures and memory
4. Memory interfacing to Programmable DSP devices

UNIT-I

Introduction to Digital Signal Procesing: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX Processors, Memory space, Program Control, Instructions and Programming, On-Chip Peripherals, Interrupts and Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Implementations of Basic DSP Algorithms: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a COURSE CODEC interface circuit, COURSE CODEC programming, A COURSE CODEC-DSP interface example.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, *Digital Signal Processing*, Thomson Publications, 2004.
2. Lapsley et al, *DSP Processor Fundamentals, Architectures & Features,* S. Chand & Co, 2000.

REFERENCES:

1. Jonathan Stein, *Digital Signal Processing*, John Wiley, 2005.
2. B. Venkata Ramani and M. Bhaskar, *Digital Signal Processors, Architecture, Programming and Applications*, TMH, 2004.

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	L	T	P	C
M.Tech - II Semester - DECS	**3**	**1**	**0**	**4**

(15BDE12) DETECTION AND ESTIMATION OF SIGNALS

Objectives:

To enable the students

1. *To understand the detection theory.*
2. *To understand the binary decision – multiple observations.*
3. *To understand the estimation theory.*
4. *To understand the prediction .*

Outcomes:

The student will

1. *Understand the various decision criterion.*
2. *Understand the various methods of estimation.*
3. *Understand the properties of estimators.*
4. *Understand the statistical estimation of parameters.*

UNIT I

DETECTION THEORY: Binary decisions - Single observation- Maximum likelihood decision criterion, Neymann-Pearson criterion, Probability of error criterion, Bayes risk criterion, Minimax criterion, Robust detection, Receiver operating characteristics.

UNIT II

BINARY DECISIONS - MULTIPLE OBSERVATIONS: Vector observations, the general Gaussian Problem, Waveform Observation in Additive Gaussian Noise, The Integrating Optimum Receiver; Matched Filter Receiver.

UNIT III

ESTIMATION THEORY: Methods -Maximum likelihood estimation; Bayes cost method Bayes estimation criterion - Mean square error criterion; Uniform cost function; absolute value cost function; Linear minimum variance - Least squares method; Estimation in the presence of Gaussian noise - Linear observation; Non-linear estimation.

UNIT IV

PROPERTIES OF ESTIMATORS: Bias, Efficiency, Cramer Rao bound Asymptotic properties, Sensitivity and error analysis.

UNIT V

STATE ESTIMATION: Prediction, Kalman filter.

SUFFICIENT STATISTICS AND STATISTICAL ESTIMATION OF PARAMETERS: Concept of sufficient statistics, Exponential families of Distributions, Exponential families and Maximum likelihood estimation, uniformly minimum variance unbiased estimation.

TEXT BOOKS:

1. James L. Melsa and David L. Cohn, "Decision and Estimation Theory," McGraw Hill, 1978.
2. Dimitri Kazakos, P. Papantoni Kazakos, "Detection and Estimation," Computer Science Press, 1990.
3. Steven M. Kay, "Statistical Signal Processing: Vol. 1: Estimation Theory, Vol. 2: Detection Theory," Prentice Hall Inc., 1998.

REFERENCES:

1. Jerry M. Mendel, "Lessons in Estimation Theory for Signal Processing, Communication and Control," Prentice Hall Inc., 1995
2. Sophocles J. Orfanidis, "Optimum Signal Processing," 2 nd edn., McGraw Hill, 1988.
3. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling," John Wiley & Sons Inc., 1996.

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	L	T	P	C
M.Tech-II Semester-DECS	**3**	**1**	**0**	**4**

(15BDE13) COMPRESSION TECHNIQUES
(ELECTIVE – III)

Objectives

1 To learn about the various compression techniques for audio signals- video signals and text data.

2. Discuss important issues in data compression

3. Estimate the effect and efficiency of a data compression algorithm.

Outcomes:

At the completion of the course, students should be able to:

1. *Able to understand the concept of requirement for memory space reduction*
2. *Use lossless and lossy applications to compress data/multimedia*
3. *Learn how to design and implement compression algorithms.*

UNIT I

REVIEW OF INFORMATION THEORY: The discrete memoryless information source, Kraft inequality; optimal codes Source coding theorem. Compression Techniques, Lossless and Lossy Compression, Mathematical Preliminaries for Lossless Compression, Huffman Coding, Optimality of Huffman codes, Extended Huffman Coding, Adaptive Huffman Coding, Arithmetic Coding, Adaptive Arithmetic coding, Run Length Coding.

UNIT II

DICTIONARY TECHNIQUES: Static Dictionary, Adaptive Dictionary, LZ77, LZ78, LZW, Applications, Predictive Coding, Prediction with Partial Match, Burrows Wheeler Transform, Sequitur, Lossless Compression Standards (files, text, and images, faxes), Dynamic Markov Compression.

MATHEMATICAL PRELIMINARIES FOR LOSSY CODING: Rate distortion theory: Rate distortion function R(D),Properties of R(D); Calculation of R(D) for the binary source and the Gaussian source, Rate distortion theorem, Converse of the Rate distortion theorem,

UNIT III

QUANTIZATION: Uniform & Non-uniform, optimal and adaptive quantization, vector quantization and structures for VQ, Optimality conditions for VQ, Predictive Coding, Differential Encoding Schemes.

UNIT IV

MATHEMATICAL PRELIMINARIES FOR TRANSFORMS: Karhunen Loeve Transform, Discrete Cosine and Sine Transforms, Discrete Walsh Hadamard Transform, Lapped transforms- Transform coding, Subband coding, Wavelet Based Compression, Analysis/Synthesis Schemes.

UNIT V

DATA COMPRESSION STANDARDS: Zip and Gzip, Speech Compression Standards: MPEG, JPEG 2000. MPEG, H264.

IMAGE COMPRESSION STANDARDS: Binary Image Compression Standards, Continuous Tone Still Image Compression Standards, Video Compression Standards.

TEXT BOOKS:

1. Khalid Sayood, "Introduction to Data Compression", Morgan Kaufmann Publishers., Second Edn., 2005.
2. David Salomon, "Data Compression: The Complete Reference", Springer Publications, 4th Edn., 2006.
3. Thomas M. Cover, Joy A. Thomas, "Elements of Information Theory," John Wiley & Sons, Inc.,1991.

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education.
2. Ali N. Akansu, Richard A. Haddad, "Multiresolution Signal Decomposition: Transforms, Subbands and Wavelets", Academic Press., 1992
3. Martin Vetterli, Jelena Kovacevic, "Wavelets and Subband Coding", Prentice Hall Inc., 1995.

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	L	T	P	C
M.Tech-II Semester-DECS	**3**	**1**	**0**	**4**

(15BDE14) MICRO COMPUTER SYSTEM DESIGN
(ELECTIVE – III)

Objectives

1.To demonstrateaninternal architecture of advanced microprocessors.

2.Provide a strong foundation on memory hierarchy design and tradeoffs in both uniprocessor and multiprocessors.

3.To demonstrate an internal architecture of arithmetic co-processorsand its instruction set

4.To understand the fundamentals of I/O Design

Outcomes

After completing this course students should be able to:

1. Explain the internal architecture of the 16, 32, and 64-bit microprocessors
2. Describe the features and use of the real and protected modes of microprocessors.
3. Compare and contrast the features of different members of an advanced microprocessors family.(The INTEL family).
4. Understand the architecture of arithmetic co-processors

UNIT I

REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures, 80186 Architecture.

UNIT II

THE 80286, 80386 AND 80486 MICRO PROCESSORS: Architectures, Register Organization, Addressing Modes andinstruction sets of 80286 (brief treatment only),Memory management,The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT III

INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Virtual Memory Concept of 80286 and other advanced Processors.

I/O PROGRAMMING: Fundamentals of I/O Considerations, Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

UNIT IV

ARITHMETIC CO-PROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment)

UNITV

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

TEXTBOOKS:

1. Barry, B. Brey, "The Intel Microprocessors,"8th Edition Pearson Education, 2009.
2. A.K. Ray and K.M. Bhurchandi,"Advanced Microprocessor and Peripherals," TMH.
3. Douglas V. Hall, "Microprocessors and Interfacing," Special Indian Edition, 2006.

REFERENCES:

1.YU-Chang, Glenn A. Gibson, "Micro Computer Systems: The 8086/8088 Family Architecture, Programming and Design" 2nd Edition, Pearson Education, 2007.
2. Walter A.triebel &Avatar Singh," the 8086 and 8088 Microprocessors"-PHI, 4 th Edition, 2003
3. A.P.Godse and D.A.Gods, "Eicroprocessors and Interfacing"-Technical Publicatios pune,1st Edition 2008

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	L	T	P	C
M.Tech-II Semester- DECS	**3**	**1**	**0**	**4**

(15BVL13) NANO ELECTRONICS
(ELECTIVE – III)

Objectives:

To enable the students

1. *To understand carbon based nano structures and their properties and application*
2. *To understand the fabrication of nanofilms with various methods*
3. *To understand the carbon based devices.*
4. *To understand how nanoelectronic devices can be used in electronic applications such as logic memory & mass storage devices..*

Outcomes:

On completion of course The student will be able to

1. *To understand various methods to fabricate.*
2. *To measure nanoscale features*
3. *To attain knowledge mass storage device*
4. *To understand data transimission*

UNIT I

NANO TECHNOLOGY AND SCIENCE:

Introduction, Nano film deposition techniques, Magnetron sputtering, Laser Ablation, Molecular beam epitaxy deposition, Lithography, Material Removing Technologies, Chemical Etching , Mechanical Processing, Scanning Probe Techniques. Carbon nano structures: C_{60} and Fullerence, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II

LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III

RADOM ACESS MEMORIES: High Permitivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT IV

MASS STORAGE DEVICES:

Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V

DATA TRANSIMISSION, INTERFACES AND DISPLAYS:

Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:

1. Rainer Waser, "Nano Electronics and Information Technology", Wiley VCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Interscience, May 2003

Reference Books:

1. George W. Hanson, "Fundamentals of Nano electronics", 2009
2. Mitin, "Introduction To Nano electronics Science, Nanotechnology, Engineering, And Applications", 2010

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M.Tech- II Semester-DECS	**3**	**1**	**0**	**4**

(15BDE15) HIGH SPEED NETWORKS
(ELECTIVE-IV)

Objectives:

1. will get an introduction about ATM and Frame relay.
2. will be provided with an up-to-date survey of developments in High Speed Networks.
3. to know techniques involved to support real-time traffic and congestion control.
4. will be provided with different levels of quality of service to different applications.

Outcomes:

After completion of this course the student will be able to:

1. design the different technologies involved in High Speed Networking and their performance.
2. Understand switching in ATM and Frame Relay networks.
3. Develop an in-depth understanding, in terms of architecture, protocols and applications of major high-speed networking technologies.
4. Solve numerical or analytical problems *pertaining to the high-speed networking technologies.*

UNIT I

NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture, QOS in IP networks: differentiated and integrated services.

UNIT II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III

ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections, QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT IV

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage class networks.

REARRANGEABLE NETWORKS: Rearrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT V

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.

TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active.

TEXT BOOKS:

1. William Stallings, "ISDN & B-ISDN with Frame Relay", PHI.
2. Leon Garcia widjaja, "Communication Networks", TMH, 2000.
3. N. N. Biswas, "ATM Fundamentals", Adventure books publishers.

Reference Books:

1. Warland & Pravin Varaiya, "HIGH PERFORMANCE COMMUNICATION NETWORKS",Jean Hardcourt Asia Pvt. Ltd.,II Edition,2001.
2. William Stallings, "HIGH SPEED NETWORKS AND INTERNET", Pearson Education, Second Edition, 2002.
3. Abhijit S. Pandya, Ercan Sea, "ATM Technology for Broad Band Telecommunication Networks", CRC Press, New York, 2004.

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(Autonomous)	**L**	**T**	**P**	**C**
M.Tech- II Semester-DECS	**3**	**1**	**0**	**4**

(15BVL09) FPGA ARCHITECTURE & APPLICATIONS

(ELECTIVE-IV)

Objectives:

To enable the students

1. *To understand different commercially available PLDS, FPGAs.*
2. *To understand different architectures and routing technology in CPLDS and FPGAs.*
3. *To understand* FSM architectures and systems level design.
4. *To familiarize with frontend and backend design tools.*

Outcomes:

The student will

1. *know about different commercially available FPGA and CPLD architectures.*
2. *design logic blocks using optimization techniques.*
3. *Understand the top down design of digital circuits.*
4. *know about mentor graphics EDA tool.*

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for FPGAs.

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. **REALIZATION OF STATE MACHINE:** Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming.Linked State Machines, One – Hot State Machine, Petrinets for State Machines – Basic Concepts, Properties. Extended Petrinets for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT IV

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT V

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Parallel Adder Cell, Parallel Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall , 1994.
2. Stephen M Trimberger, Field Programmable Gate Array Technology, Springer international Edition, 2007.
3. Stephen D Brown, R.Francis, J.Rose, Z.Vranesic, Field Programmable Gate Array, Springer, 1992.

REFERENCES:

1. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons,2008.
2. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes,2008.

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M.Tech- II Semester-DECS	**L**	**T**	**P**	**C**
	3	**1**	**0**	**4**

(15BDE16) NEURAL NETWORKS AND FUZZY LOGIC
(ELECTIVE-IV)

Objectives:

To enable the students

1. Concepts of Artificial Neural Networks;
2. Classification of neural network;
3. Implementation and applications of neural networks;
4. Concepts of fuzzy logic systems;

Outcomes:

The student will be

1. Demonstrate in depth knowledge on Neural networks and Fuzzy Systems.
2. Design and implement neural networks and neuro-fuzzy systems for particular problem.
3. Apply and evaluate Neural networks and Fuzzy Systems in communication engineering.
4. familiarize with applications of neuro-fuzzy systems.

UNIT I

FUNDAMENTAL CONCEPTS OF ANN: Historical development of Neural Networks, Biological neuron, Artificial neuron, Activation functions in ANN, Architectures of ANN, McCulloch-Pitts neuron model, Supervised and unsupervised learning, learning rules: Hebbian, Perceptron, Winner- takes-all, Out-star. Concept of linear separability.

UNIT II

FEED FORWARD AND FEEDBACK ANN: Back propagation NN: Introduction, delta learning rule, training algorithm. ADALINE architecture, LMS algorithm, Self Organizing Feature Maps(SOFM): topology, training algorithm. Learning Vector Quantization(LVQ): architecture, training algorithm. Discrete -time Hopfield Networks: architecture, training algorithm. Full Counter Propagation Networks: architecture, training algorithm, Basic concepts of associative memory: auto and hetero associative memory.

UNIT III

HARDWARE IMPLEMENTATION AND APPLICATIONS OF ANN: Neurocomputing hardware requirements, digital and analog electronic neurocomputing circuits, integrated circuit synaptic connections: voltage controlled Weights, analog storage of adjustable weights, digitally programmable weight, learning weight implementation.
Applications: Adaptive noise cancellation, Real time data compression.

UNIT IV

FUZZY LOGIC SYSTEMS: Crisp sets, fuzzy sets, operations on fuzzy sets, fuzzy relations and compositions. linguistic variables, types of membership functions, block diagram of fuzzy logic system, fuzzification, fuzzy rule base, fuzzy reasoning, defuzzification methods: centroid, weighted average method, center of sums.

UNIT V

NEURO–FUZZY MODELING AND APPLICATIONS: Introduction to Neuro-Fuzzy systems, Adaptive Neuro Fuzzy Inference System(ANFIS): architecture, hybrid learning algorithm, ANFIS as universal approximator. Applications: Printed character recognition, Channel equalization.

TEXT BOOKS:

1.Jacek M. Zurada, "Introduction to Artifical Neural Systems", JAICO Publishing House, 2006.
2.Timothy J. Ross, "Fuzzy Logic with Engineering Applications", 3rdedition,Wiley India Pvt. Ltd., 2011.
3.Jyh-Shing Roger Jang, Chen-Tsai Sun and Eiji Mizutani, "Neuro-Fuzzy and Softcomputing–A Computational Approach toLearning and Machine Intelligence", Prentice Hall, 1977.

REFERENCE:

1. S.N.Sivanandam, S.Sumathi,S. N. Deepa, "Introduction to Neural Networksusing MATLAB 6.0", 1st edition, Tata McGraw-Hill, 2006
2. Simon Haykin, "Neural Networks-A Comprehensive Foundation", PearsonEducation, 2001.
3. Laurene Fausett, "Fundamentals of Neural Networks", Pearson Education, 2004.

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	L	T	P	C
M.Tech- II Semester-DECS	**0**	**0**	**3**	**2**

(15BDE17) ADVANCED COMMUNICATIONS LAB

Objectives:

1. To have the basic knowledge on MATLab for Communication area.
2. To develop the code for shift keying methods.
3. To verify the performance evaluation for different channels

Outcomes:

After completion of the lab students will be able to:

1. Have the practical knowledge on fading techniques .
2. Applications of MAT Lab for research in Communication area.
3. Design and simulate the advanced communications systems.

List of Experiments

1. To simulate a basic Quaternary Phase Shift Keying (QPSK)
2. To evaluate Rayleigh and Rician multipath fading channel
3. Simulation Rayleigh Fading Channel Using Clarke's Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
4. Simulation Rayleigh Fading Channel Using Jake's Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
5. Generation of Maximal Sequences and Gold Sequences.
6. Performance Evaluation of QPSK System over Gaussian AWGN Channel.
7. Performance Evaluation of QPSK System over Rayleigh Fading Channel.
8. Equalization of Multipath Channel using LMS Algorithms.
9. Equalization of Multipath Channel using RLS Algorithms.
10. Performance Evaluation of RAKE Receiver over Slow Fading Channel

NOTE: Use Matlab / COM SIM.

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	L	T	P	C
M.Tech-IISemester-DECS	**0**	**0**	**3**	**2**

(15BDE18) ADVANCED DSP LAB

Objectives:

To enable the students

1. To familiarize with CC Studio and DSP starter kit.
2. To design a FIR filter and IIR filter.
3. To implement FIR filter and IIR filter on DSP trainer kit.
4. To estimate power spectrum using various methods.

Outcomes:

After completion of course

1. Students are able to implement FIR and IIR filters on DSP trainer kit.
2. Students are able to estimate power spectrum using various methods.
3. Students are able to implement DIT and DIF algorithms using CC Studio.

Note: Minimum 10 experiments are to be conducted

1. FIR Filter design Using Matlab
2. IIR Filter design Using Matlab
3. DIT-FFT Algorithm using CC Studio
4. DIF-FFT Algorithm using CC Studio
5. FFT of 1-D Signal using CC Studio
6. Power Density Spectrum of given Sequence using CC Studio
7. Implementation of FIR filter using DSP Trainer Kit (C-Code/ Assembly code)
8. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code)
9. Program to verify Decimation and Interpolation of a given Sequences.
10. Plot the Periodogram of a Noisy Signal and estimate PSD using Periodogram and Modified Periodogram methods
11. Estimation of Power Spectrum using Bartlett and Welch methods
12. Verification of Autocorrelation Theorem
13. Parametric methods (Yule-Walker and Burg) of Power Spectrum Estimation
14. Generation of Dual Tone Multiple Frequency (DTMF) Signals

Note: Use MATLAB and DSP Processor Kits.

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M.Tech- II Semester-DECS	**0**	**0**	**0**	**2**

(15BDE19) SEMINAR - II

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	L	T	P	C
M.Tech- II Semester-DECS	**0**	**0**	**0**	**2**

(15BDE20) COMPREHENSIVE VIVA

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	L	T	P	C
M.Tech- III & IV Semesters-DECS	**0**	**0**	**0**	**12**

(15BDE21) PROJECT WORK